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" field maintenance print set

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VT72T FIELD MAINTENANCE PRINT SET

 $B-TC-VT72T-\emptyset-2$

VT72T UNIT ASSY

 $A-PL-VT72T-\emptyset-\emptyset$

16K 16 BIT DYNAMIC READ/WRITE MEMORY

A-PL-MSV11-DC-Ø

32K 16 BIT MOS MEN

 $D-CS-M8\emptyset44-\emptyset-1$

32K 16 BIT MOS MEM

D-UA-M8Ø44-Ø-Ø

ASYN LINE INTERFACE

A-PL-DLV11-F-Ø

ASYN LINE INTERFACE

D-CS-M8Ø28-Ø-1

ASYN LINE INTERFACE

D-UA-M8Ø28-Ø-Ø

PACKAGING INSTRUCTIONS VT72/T DISPLAY

A-SP-3700364-0-0

VT72 FIELD MAINTENANCE PRINT SET

MPØØ613

VT72T/VOL 2

Field Maintenance
Print Set

Digital Equipment Corporation

PRINT SET ORDER NO. MPØØ615

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UNIT VARIATIONS

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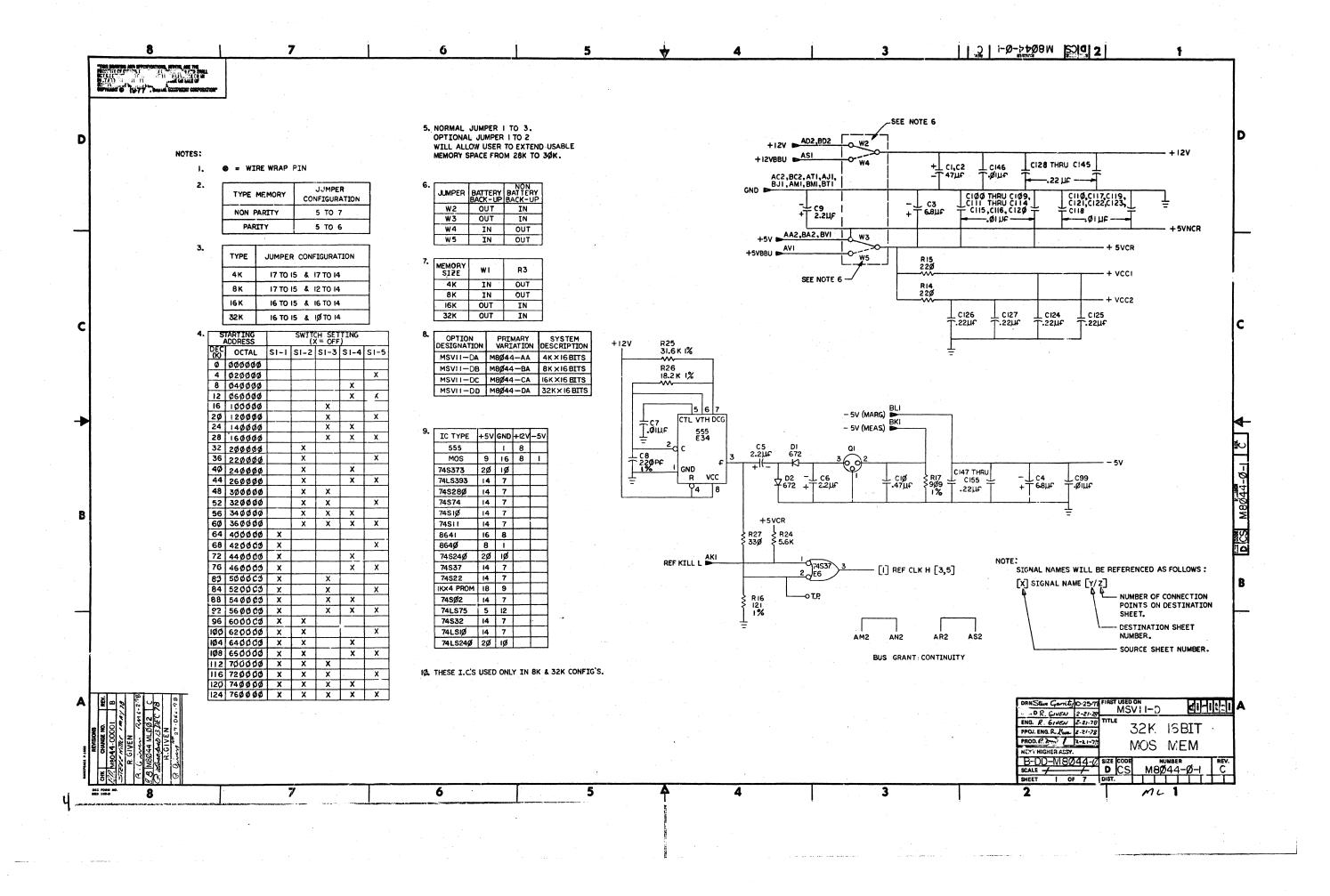
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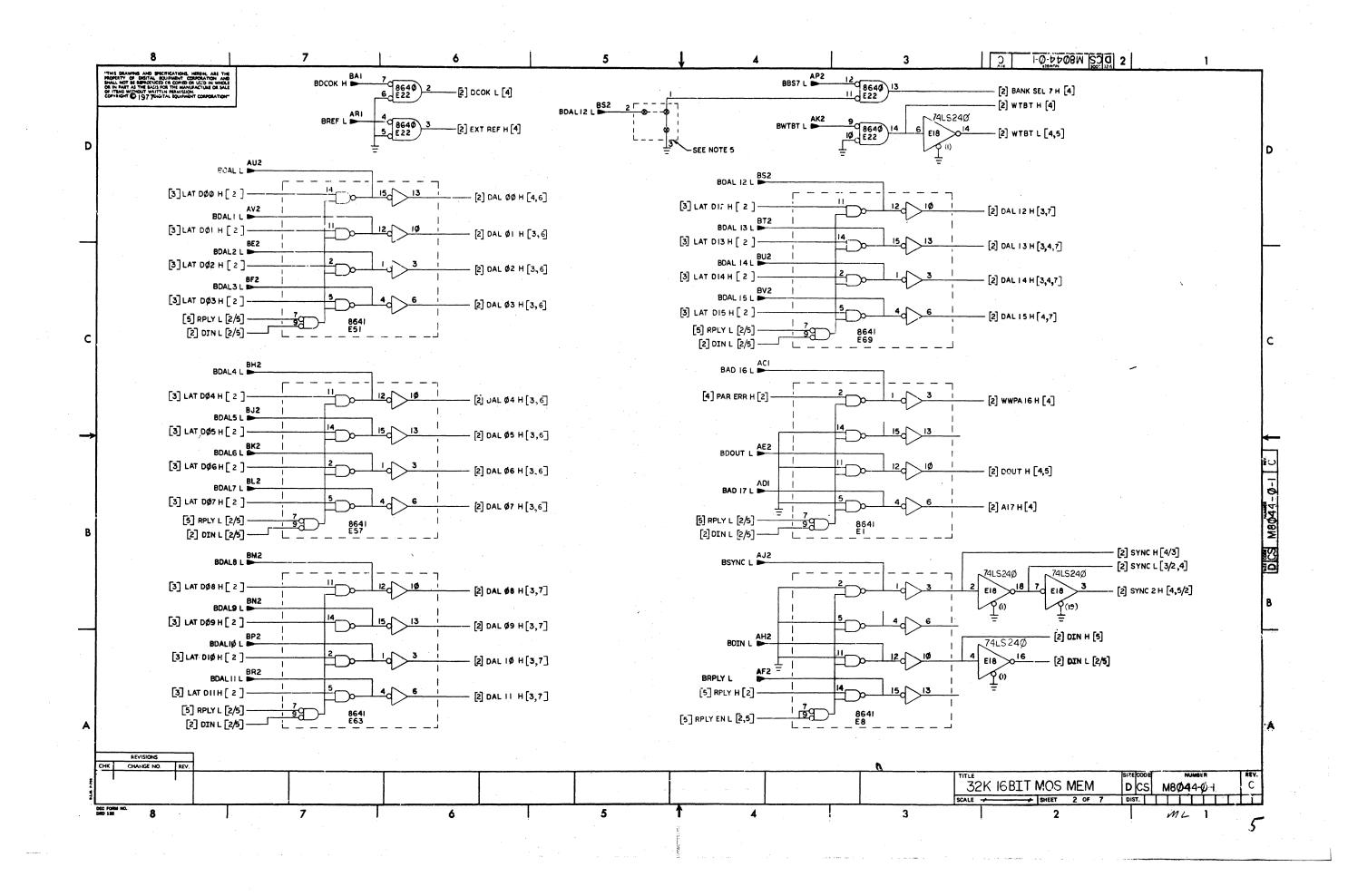
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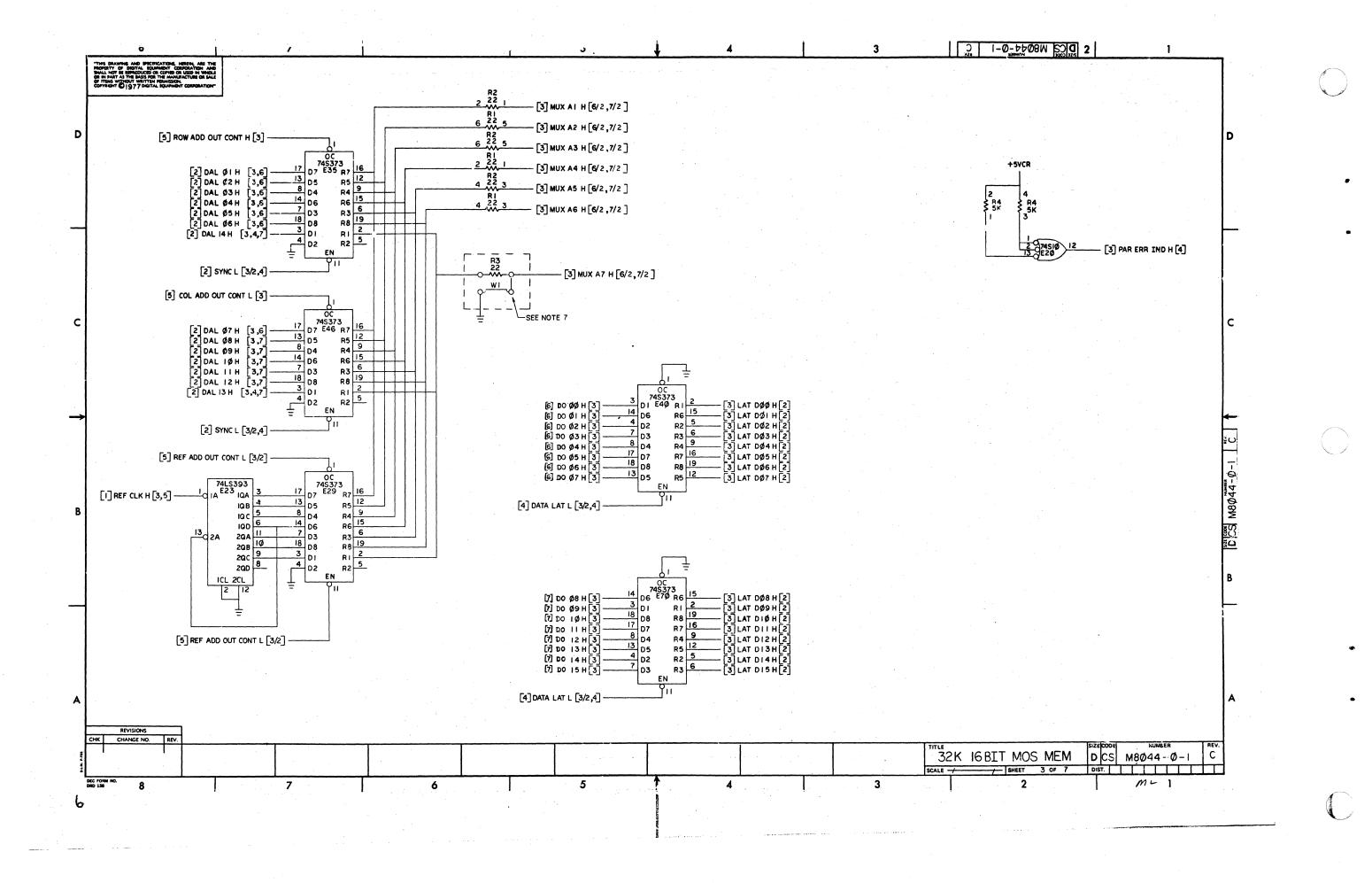
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ITEM NO.			DESCRIPTION			VT72T-	VT72	VT72	VT72						
1	E-UA-VT72-AA-Ø	VT72 BASIC AS	SY (115V/6Ø	HZ)		1	<u>-</u>	1	-						
2	E-UA-VT72-AD-Ø	VT72 BASIC AS	SY (23ØV/ 5Ø	HZ)			1	-	1						
3	A-PL-MSV11-DC	16K 16 BIT DY	NAMIC READ/W	RITE MEMORY	7	1	1_	2	2						L
4	A-PL-DLV11-F	SERIAL LINE U	NIT			1	1	1	1						
5	B-IA-7420034-Ø-Ø	LOGO VI72T				1	1	1	1						
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7	A-SP-3700364-0-0	PACKAGING INS	TRUCTIONS VT	72T DISPLAY	7	1	1	1	1			·			
8	A-PL-MRV11-VC	BOOTSTRAP				1	_	1	-						
9	A-SP-9905261-00	CARTON REG SI	OTTED WITH F	OAM		1	1	1	1						
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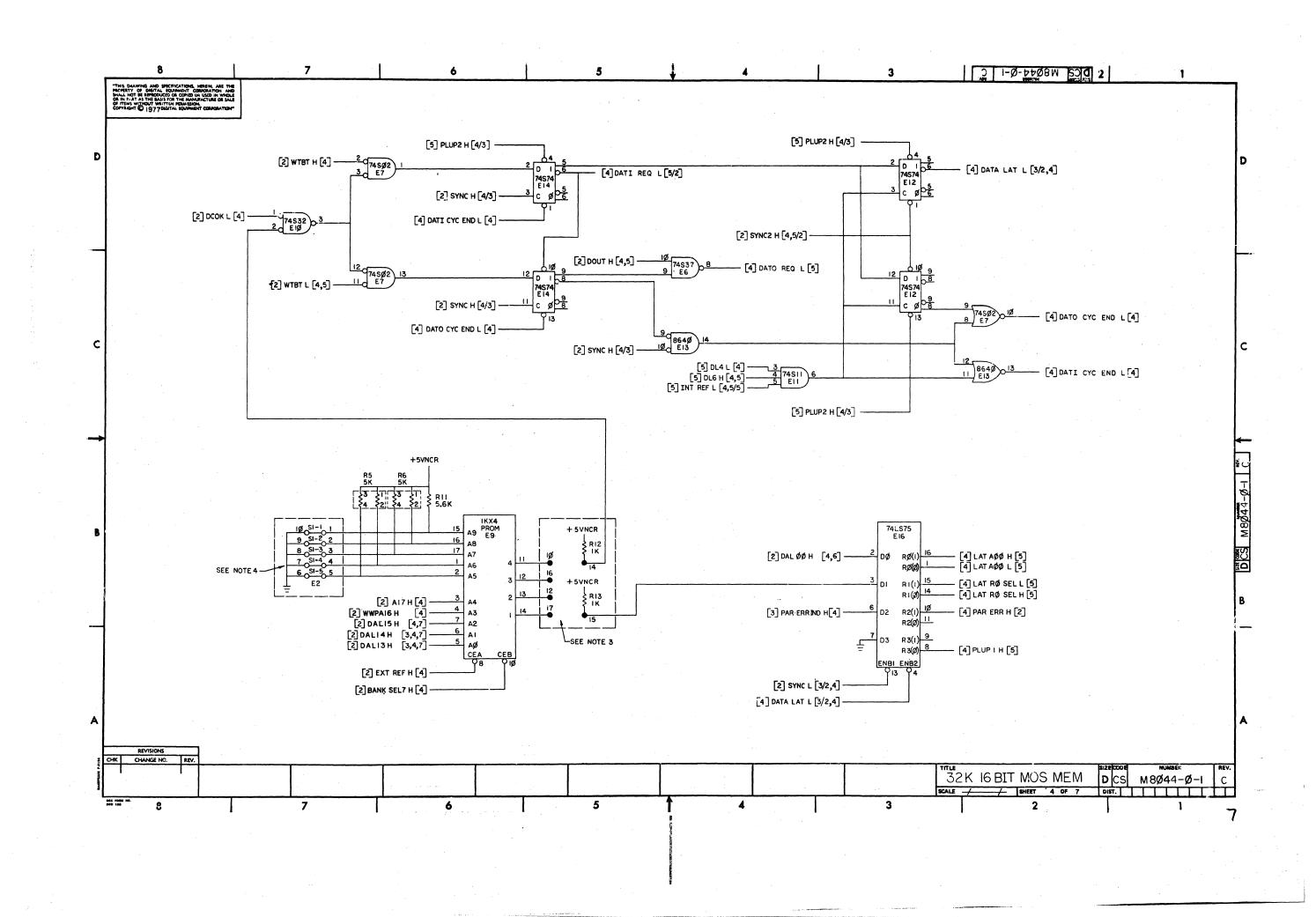
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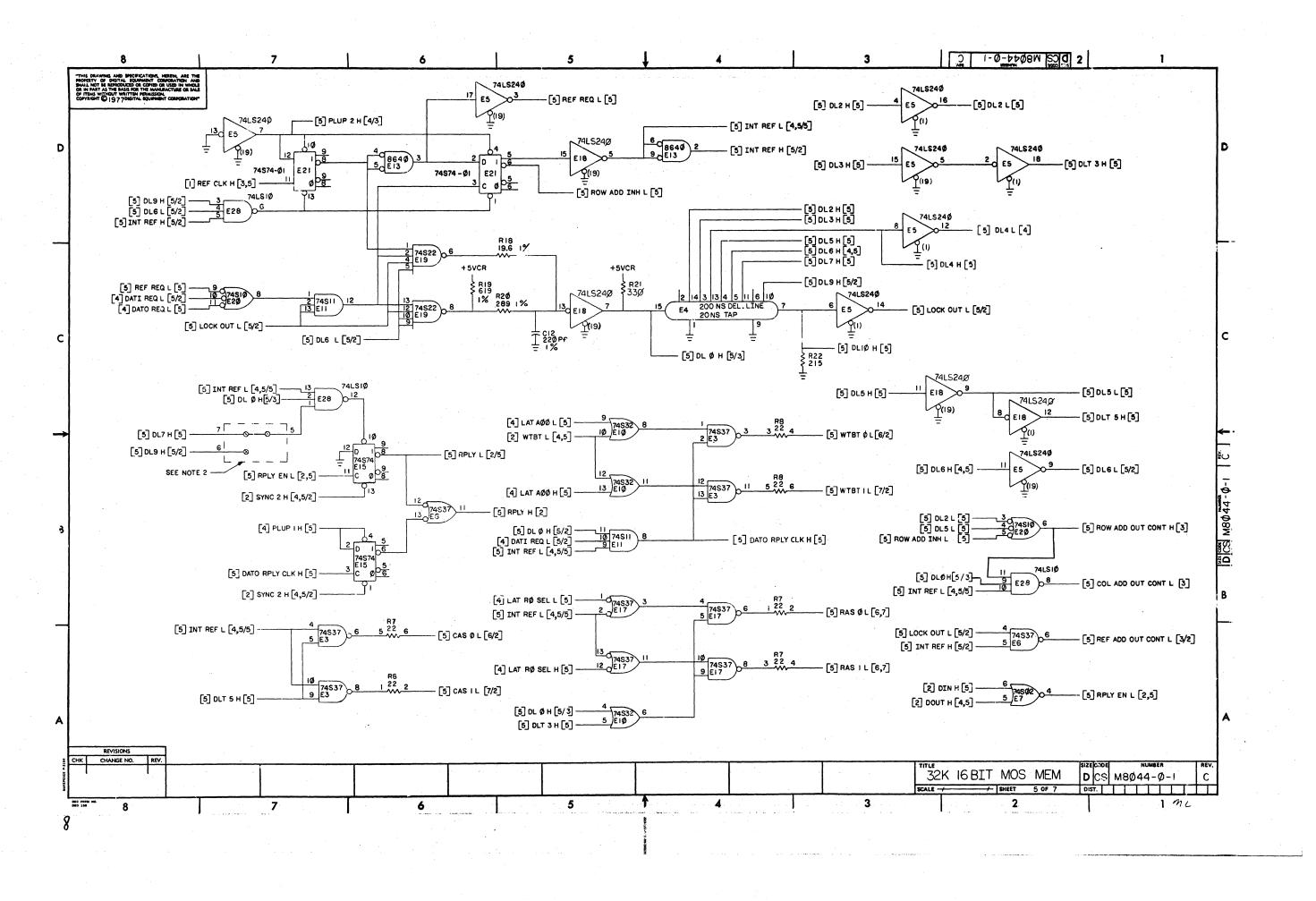
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DATE		DATE 2-21-78	ISSUED SECT.	MSV11									
NO.	DWG NO./PART NO.	DESCRIP	TION	MS									
ı	D-UA-M8Ø44-Ø-Ø	MSV11-D (32K X 16) MC	S MEMORY SYSTE	м 1									
2	D-BD-MSV11-D-4	MSV11-D/E BLOCK DIAGE	RAM	RE	F								
3	D-FD-MSV11- D -5	MSV11-D/E FLOW DIAGRA	M	RE	F			<u> </u>					
4	A-SP-MSV11-D-3	MSV11-D SYSTEM SPECIF	TICATION	RE	F								
5	D-TD-MSV11- D -6	MSV11-D/E TIMING DIAC	RAM	RE	F				<u> </u>				
6	A-PL-MSV11-D-7	MSV11-D SHIPPING LIST	·	RE	F		4	<u> </u>	<u> </u>			4_	_
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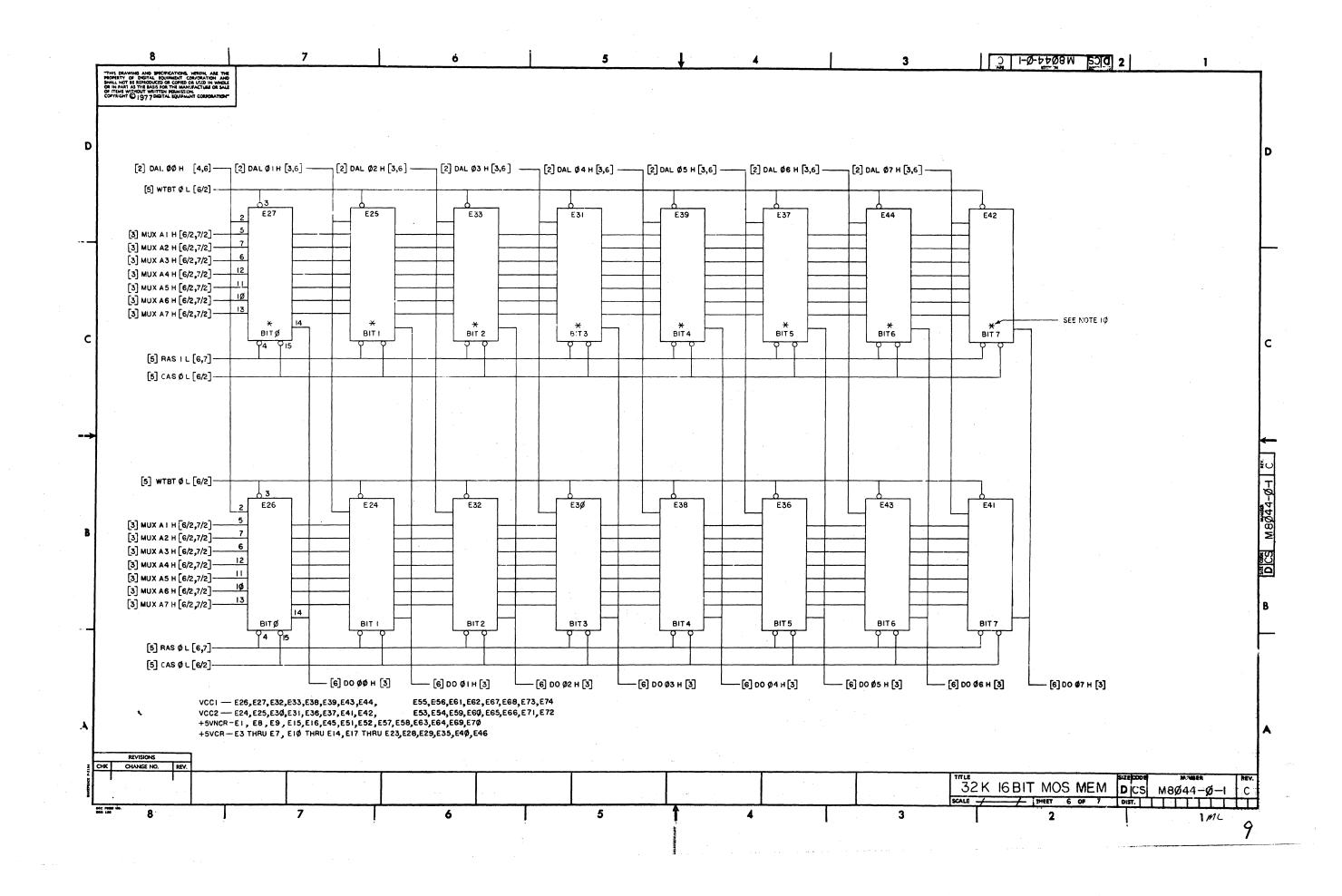


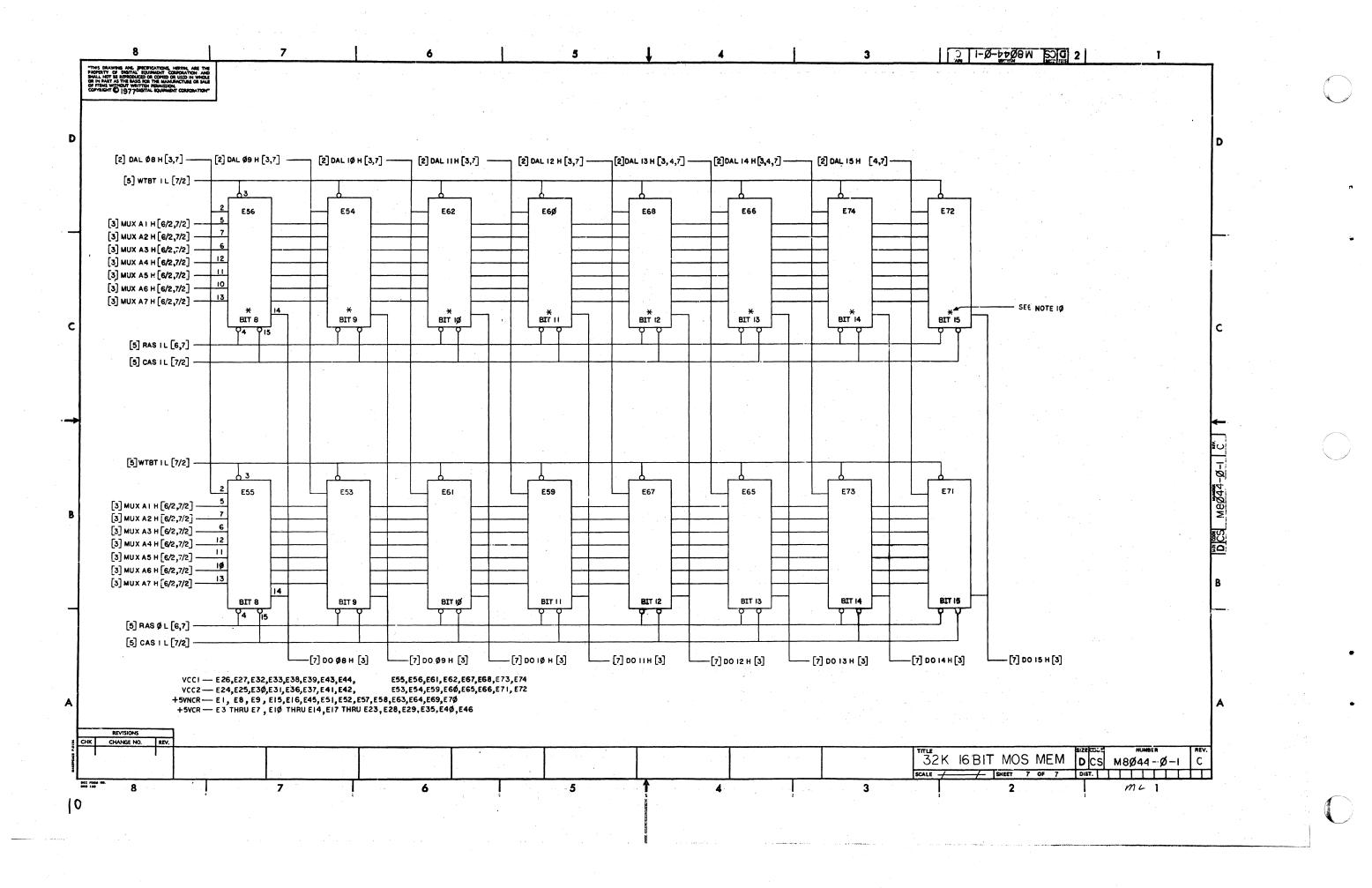


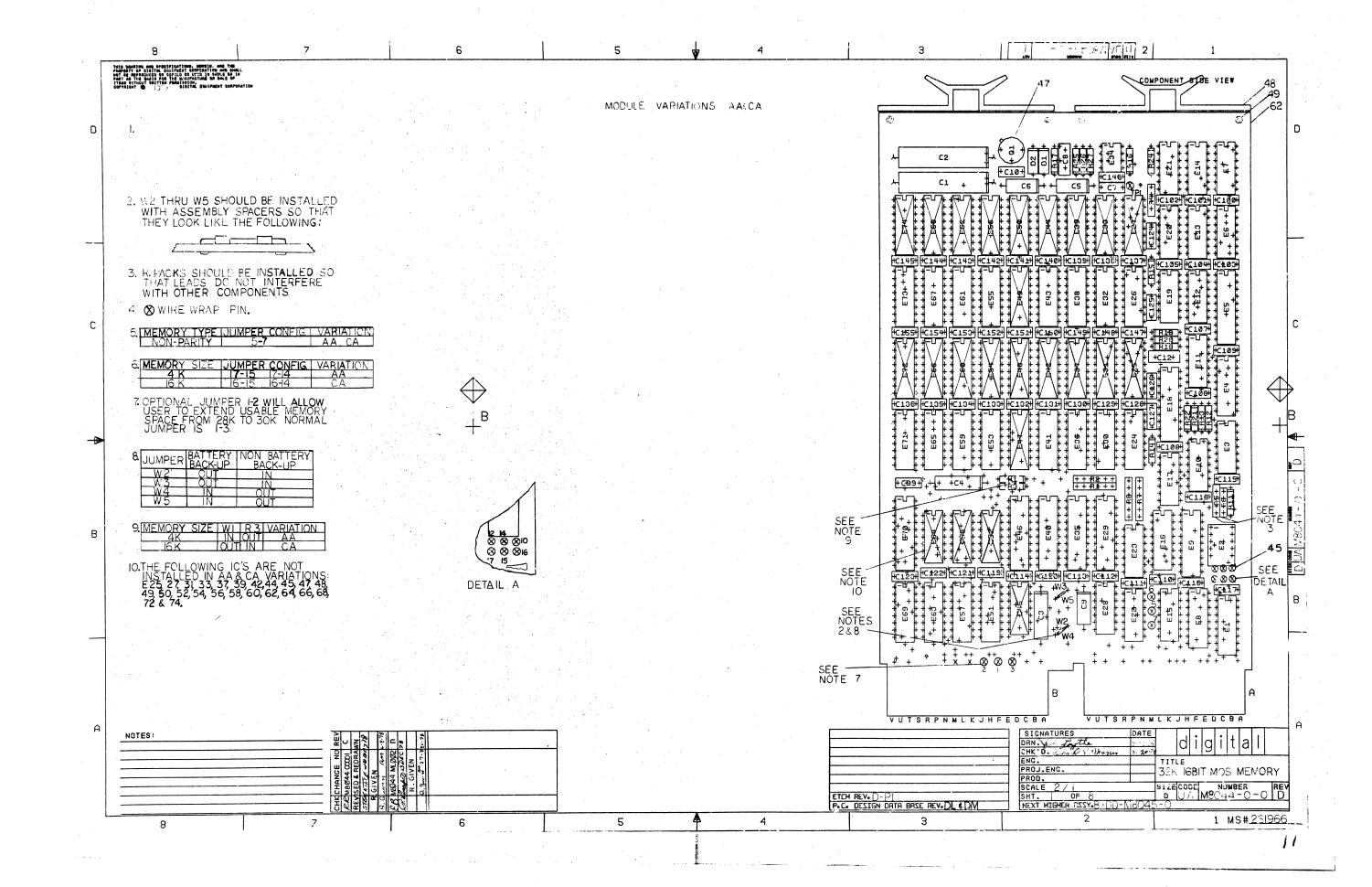


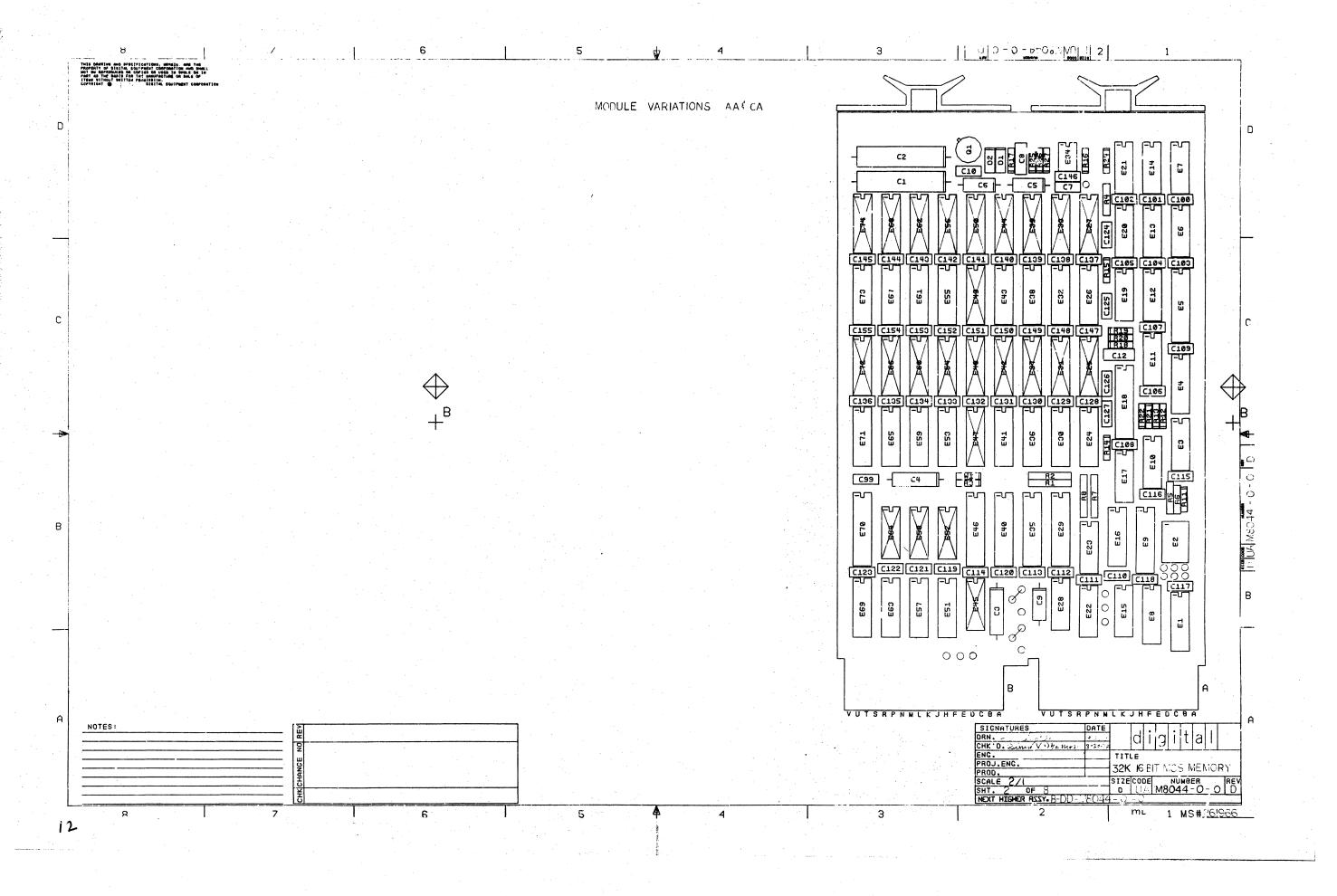


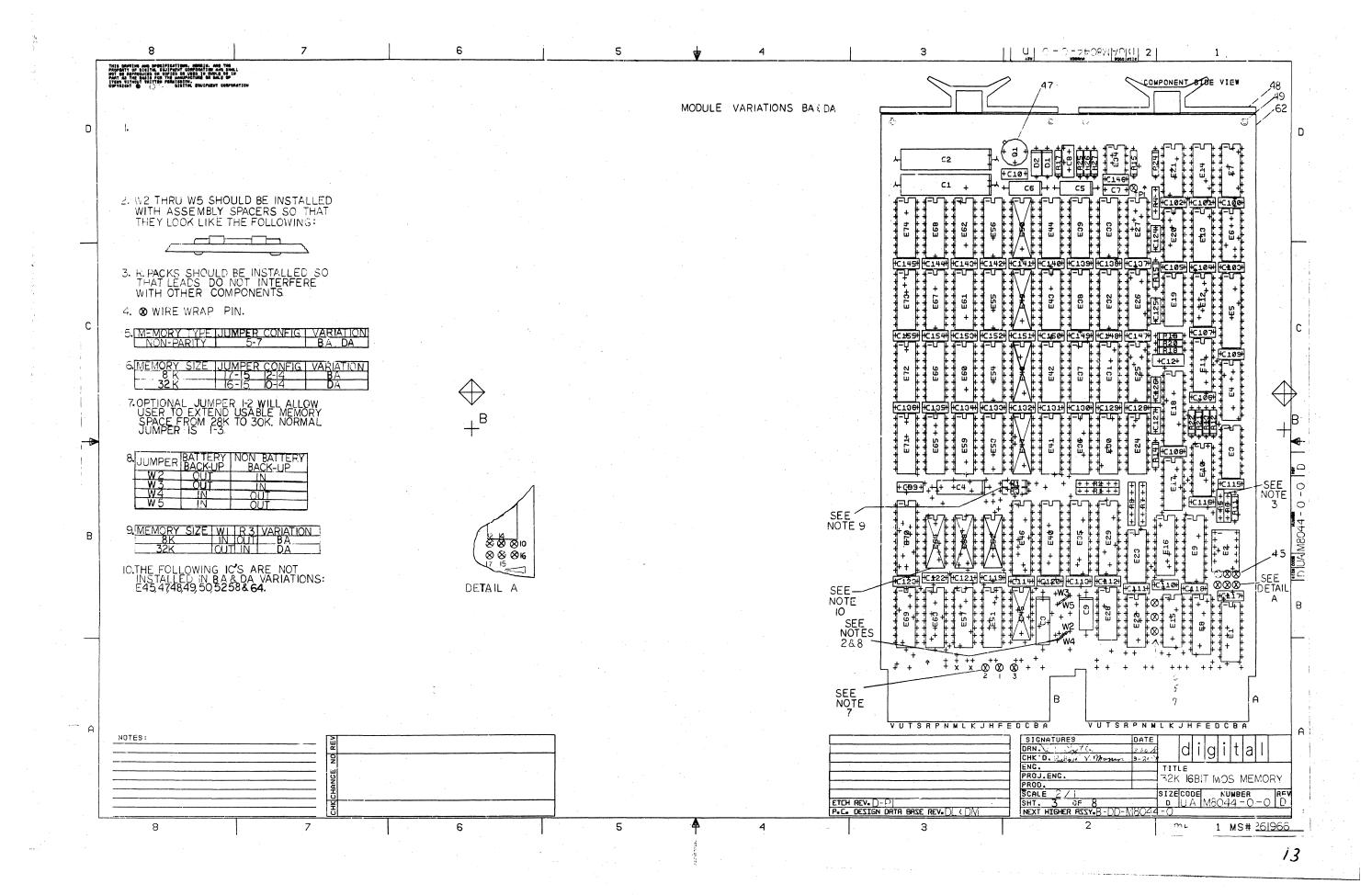
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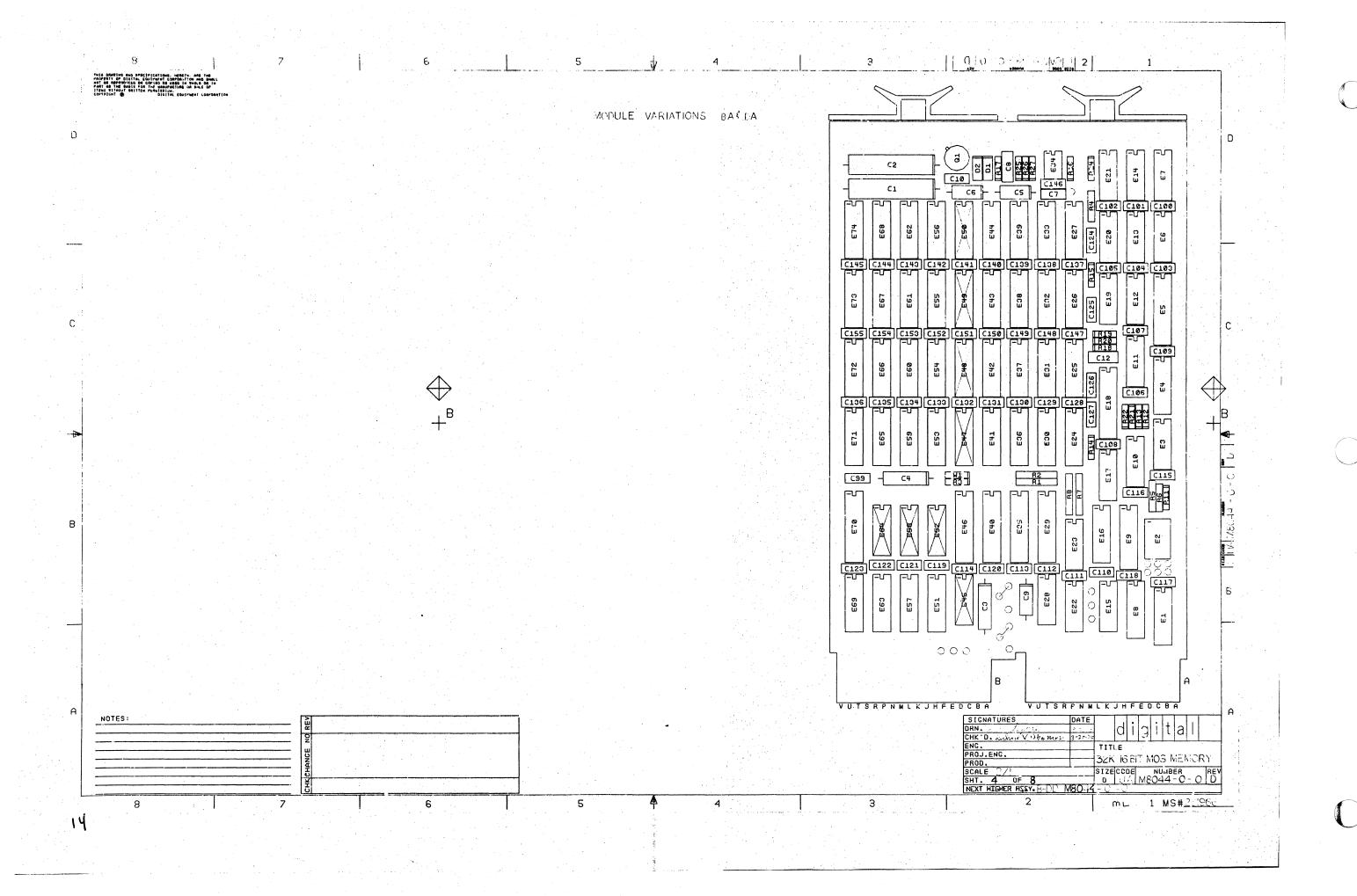


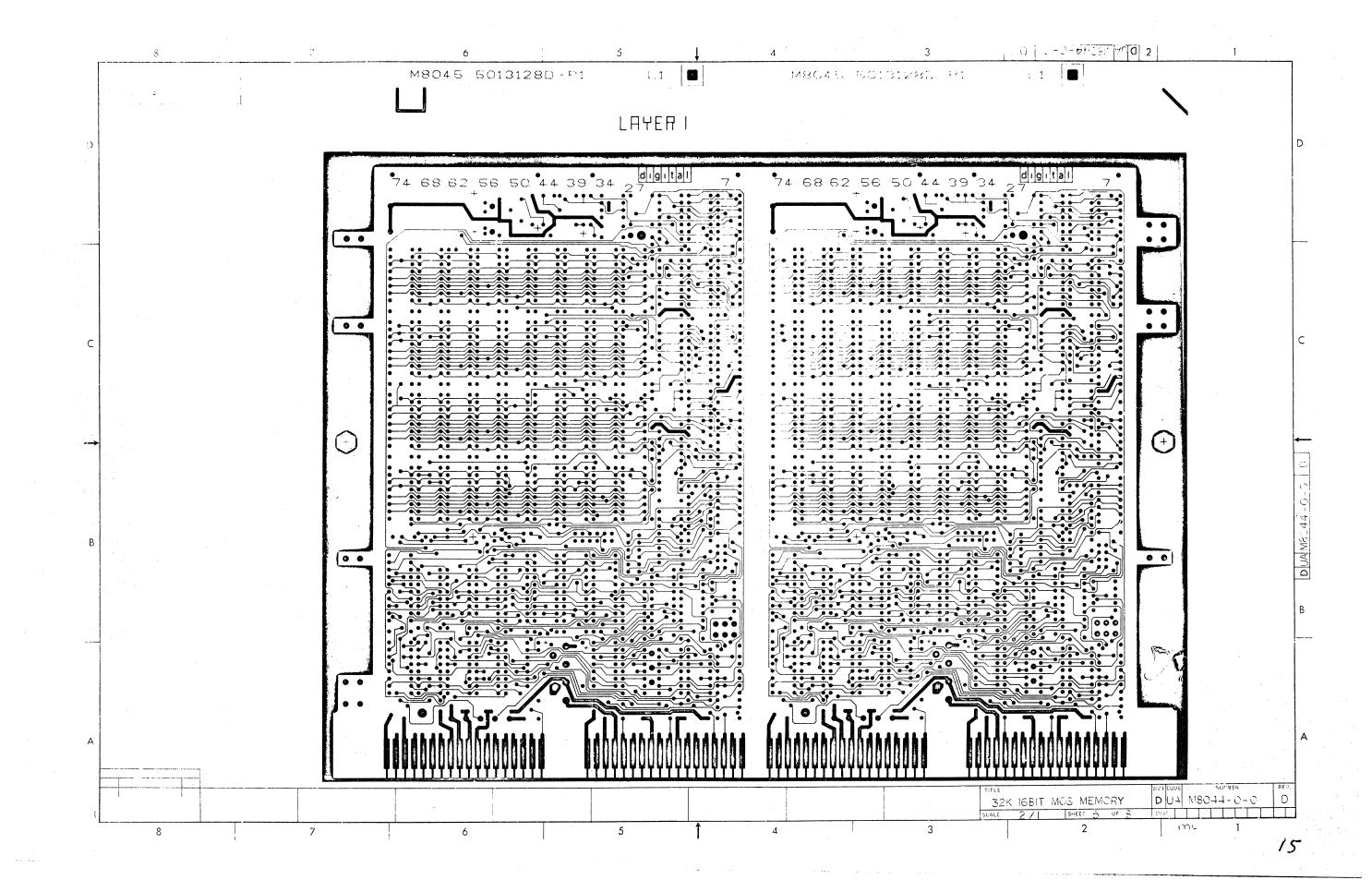








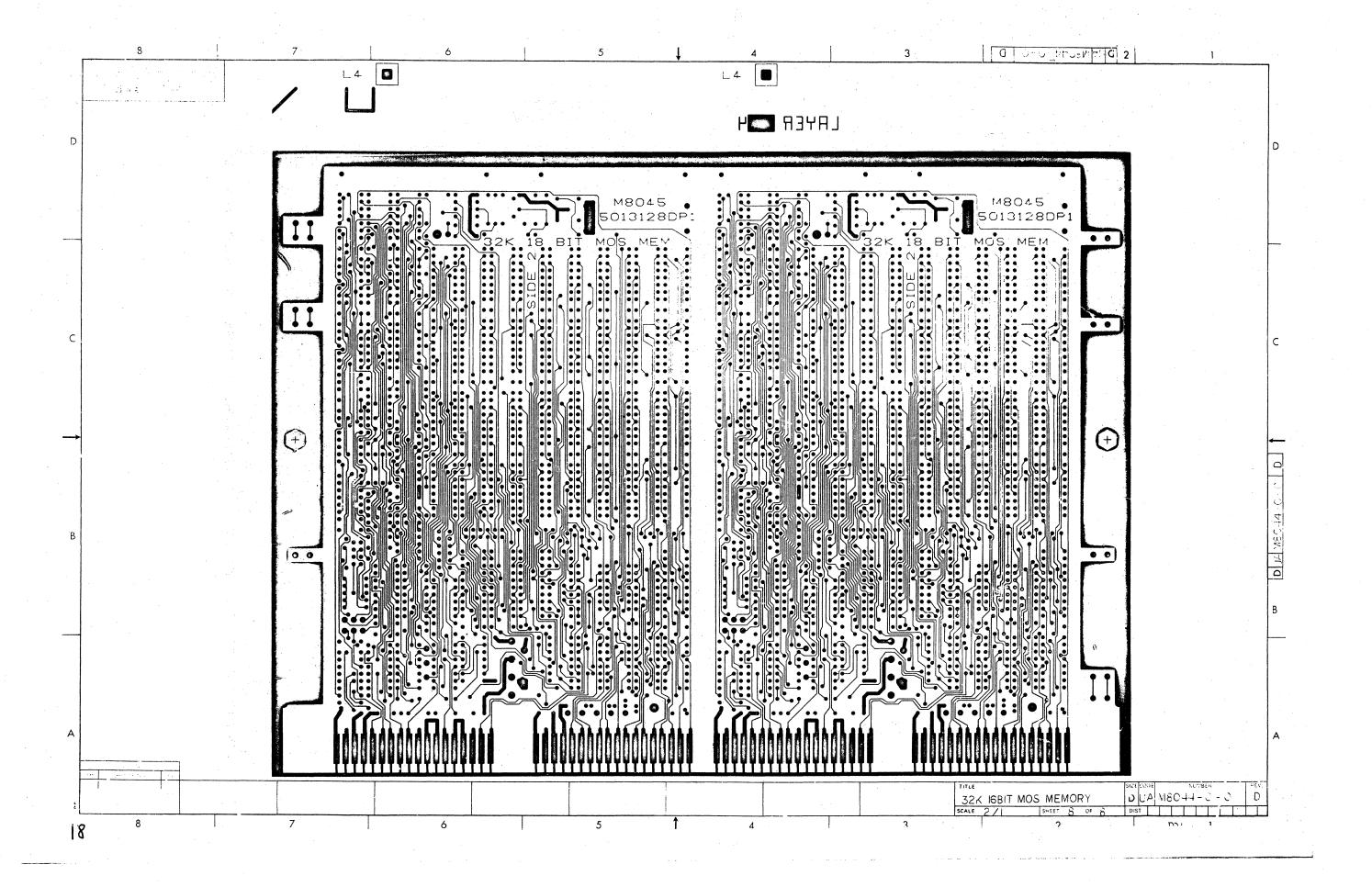




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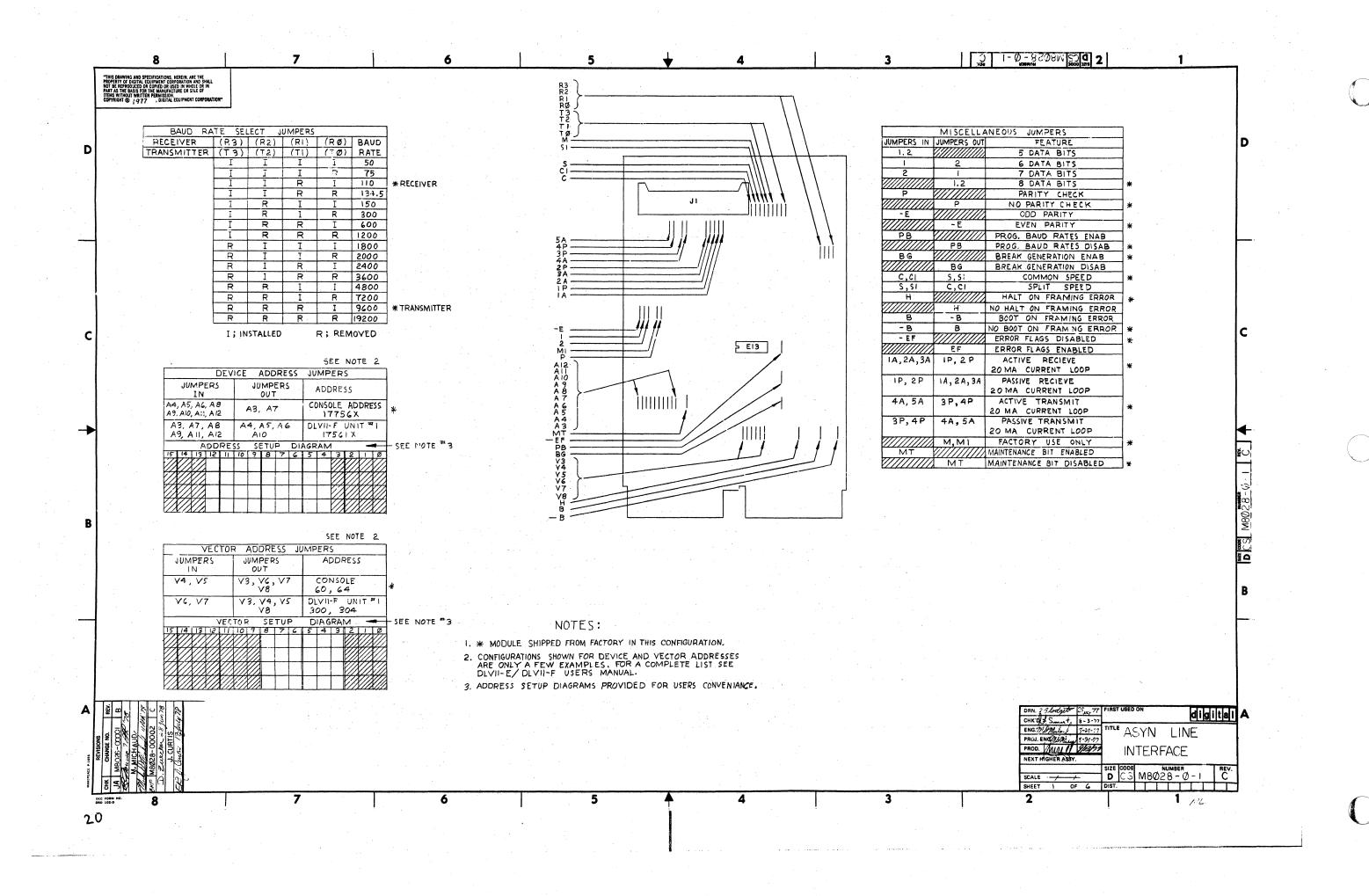
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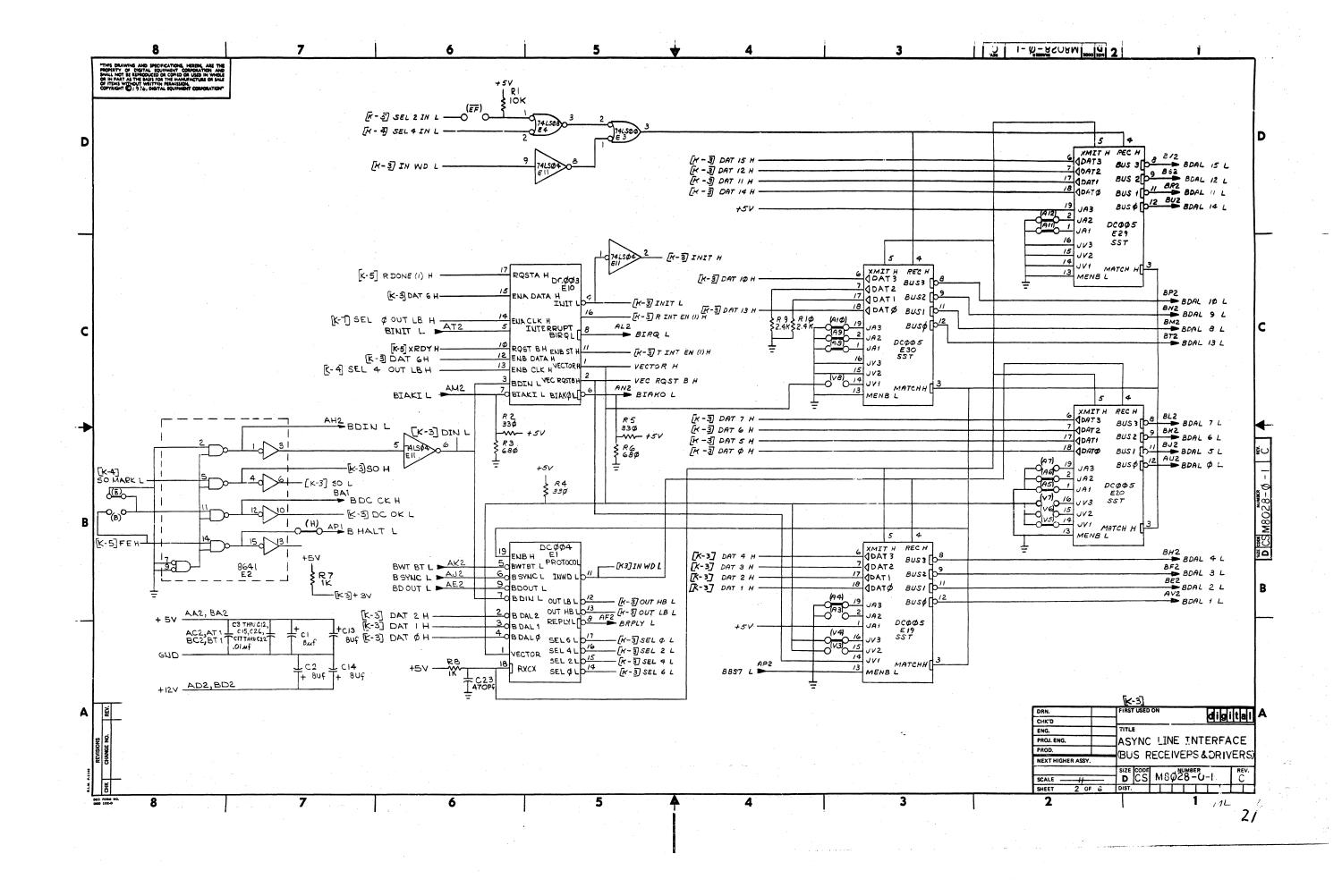


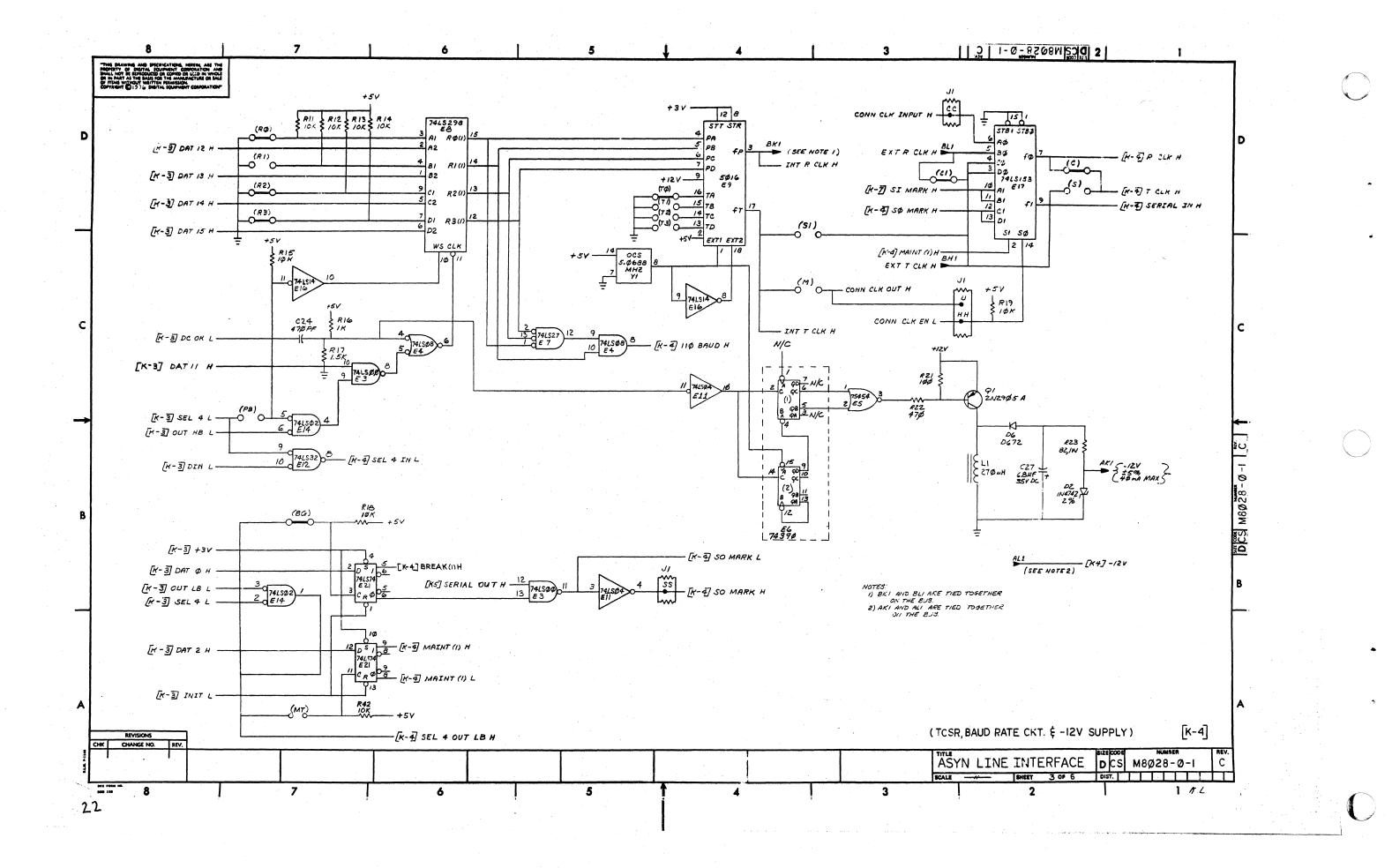
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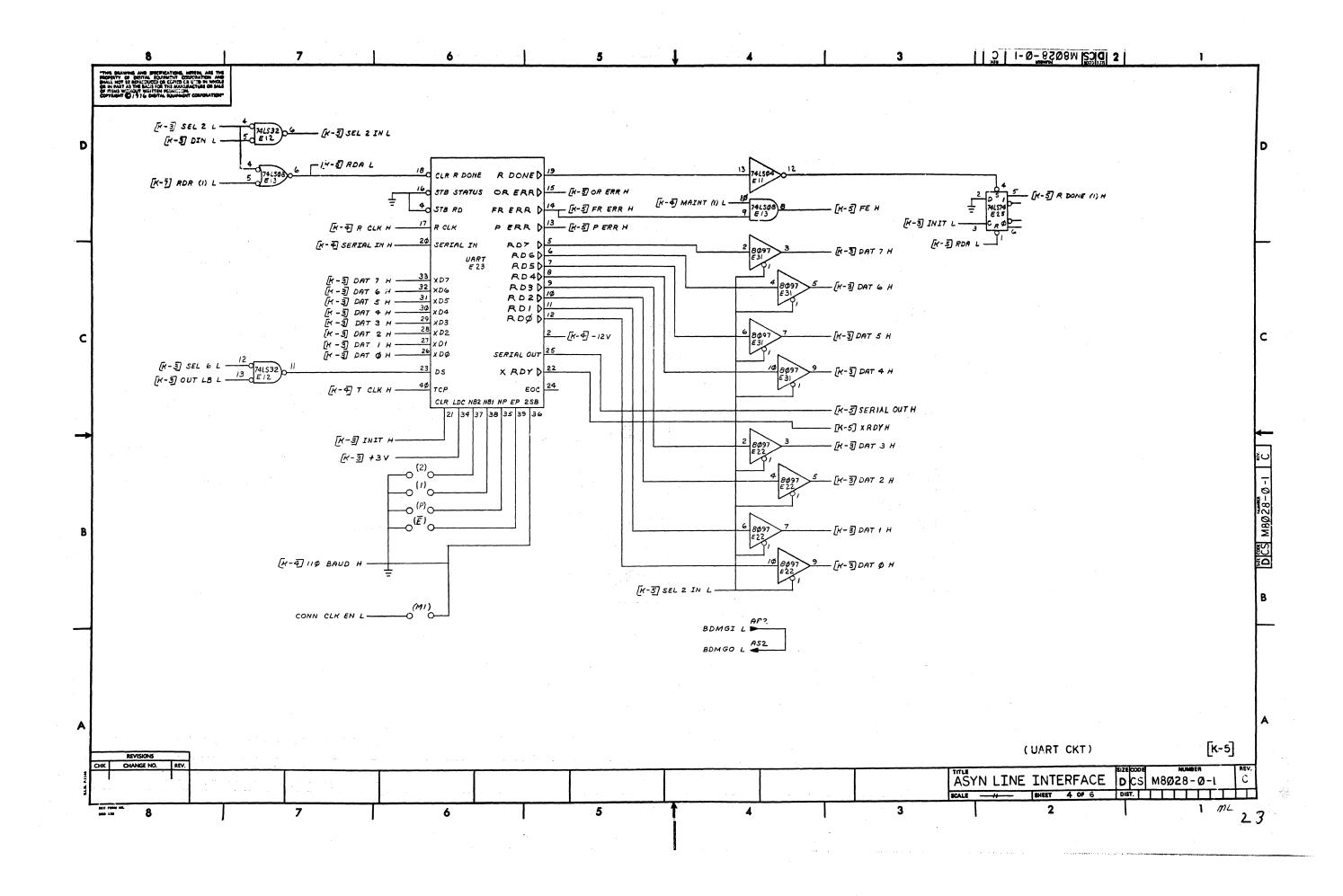
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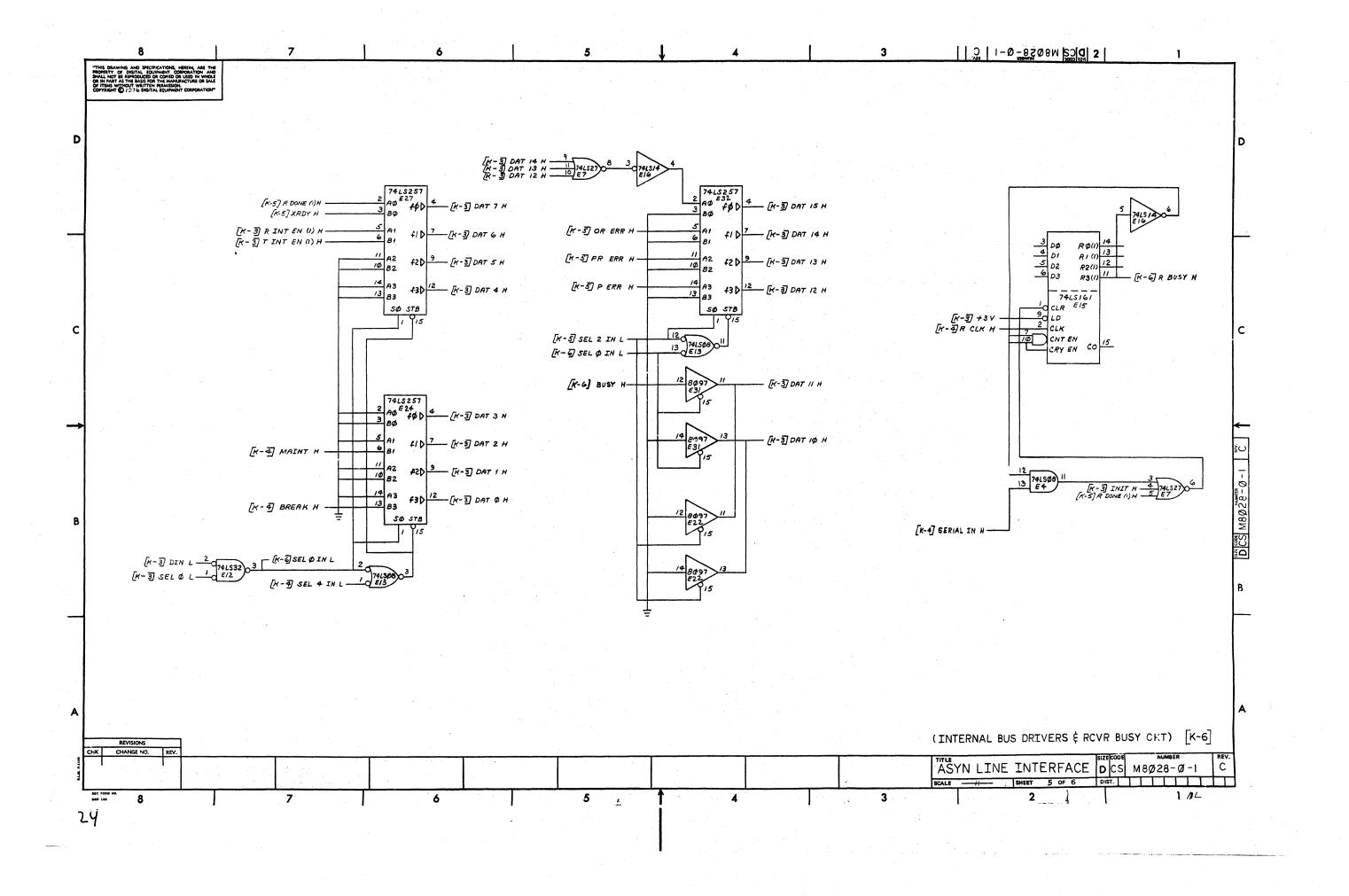
MAYNARD, MASSACHUSETTS PARTS LIST MADE BY M. MICHAUD DATE 11 AUG 77 DATE 11 AUG	
1 D-UA-M8Ø28-Ø-Ø DLV11-F ASYN LINE INTERFACE, M8Ø28 1 1 1 1 1	
2 A-SP-3700297-40 PACKAGING INSTRUCTIONS 1 1 1 1 1	
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4 D-UA-BCØ3L-Ø5 CABLE ASSEMBLY, BCØ3L-Ø5 - - - 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 <td></td>	
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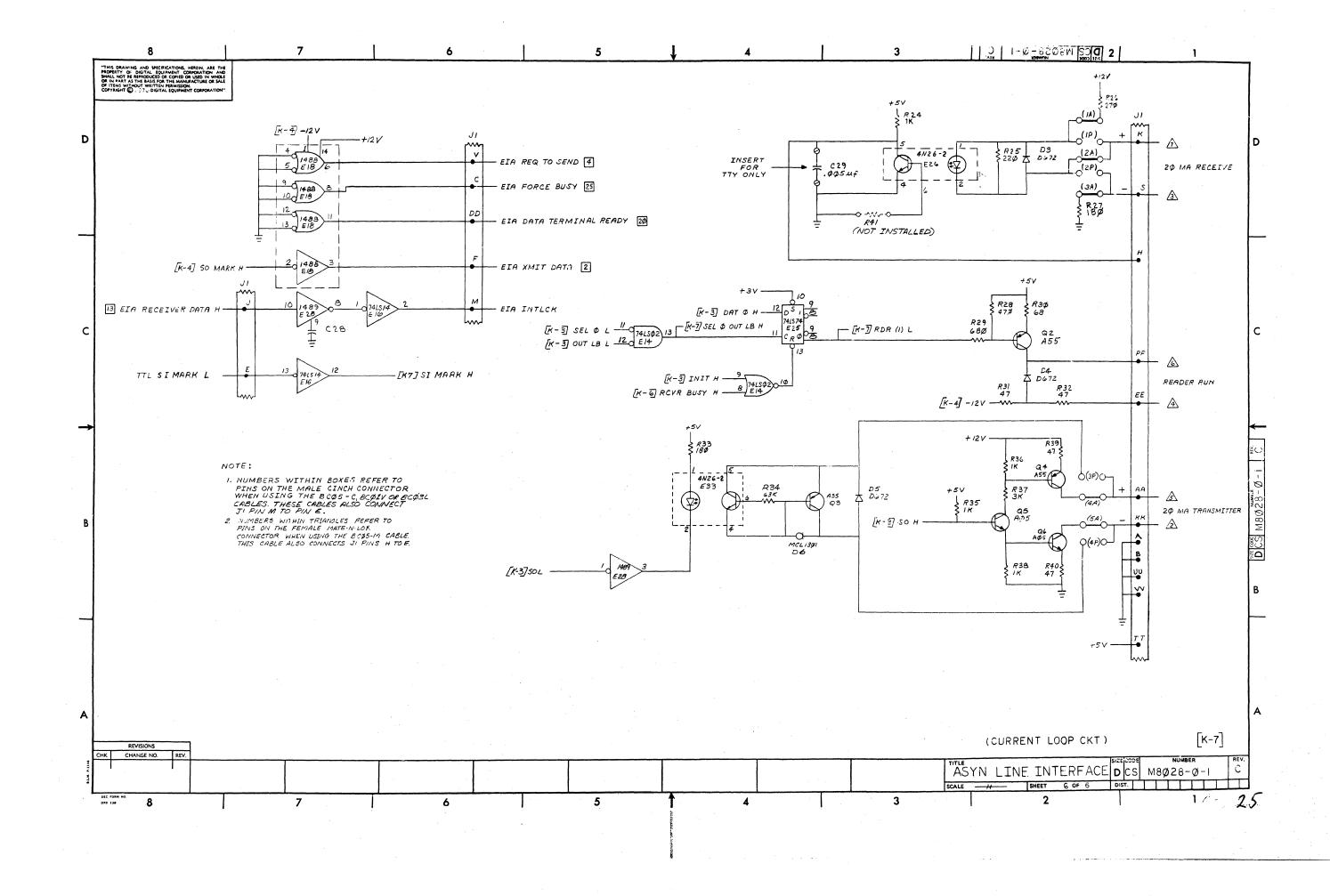


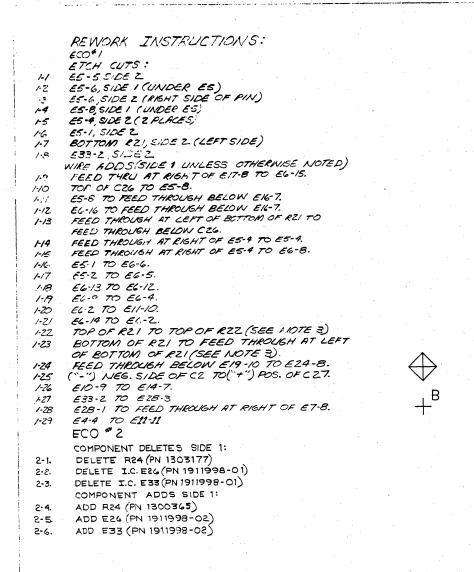




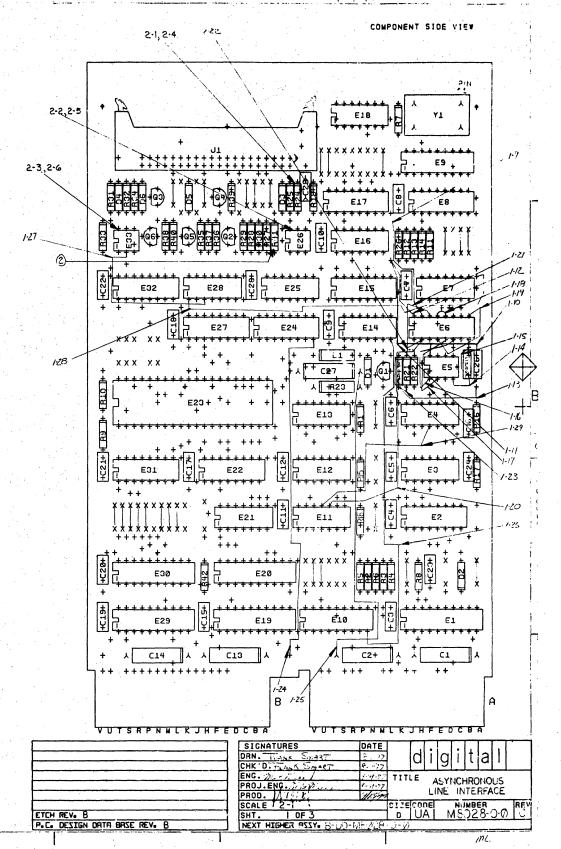


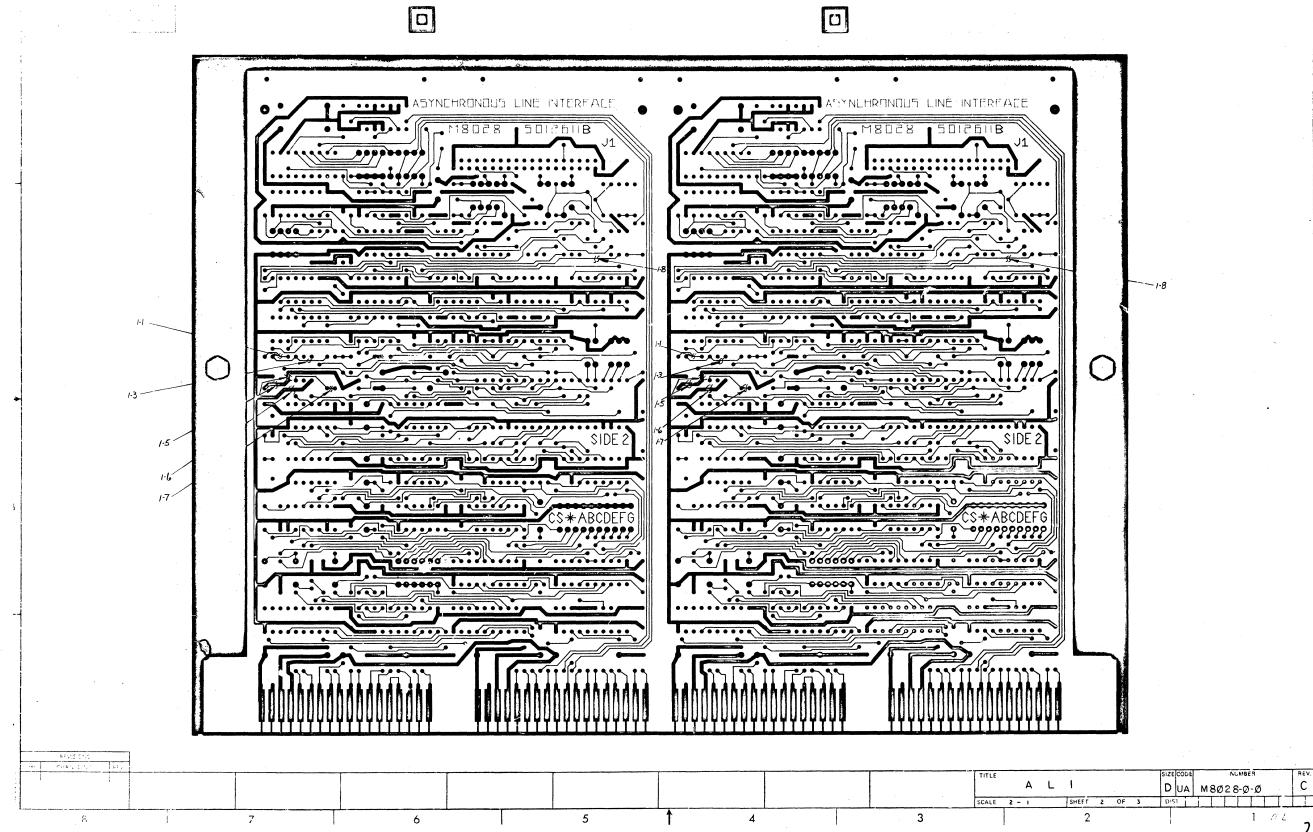




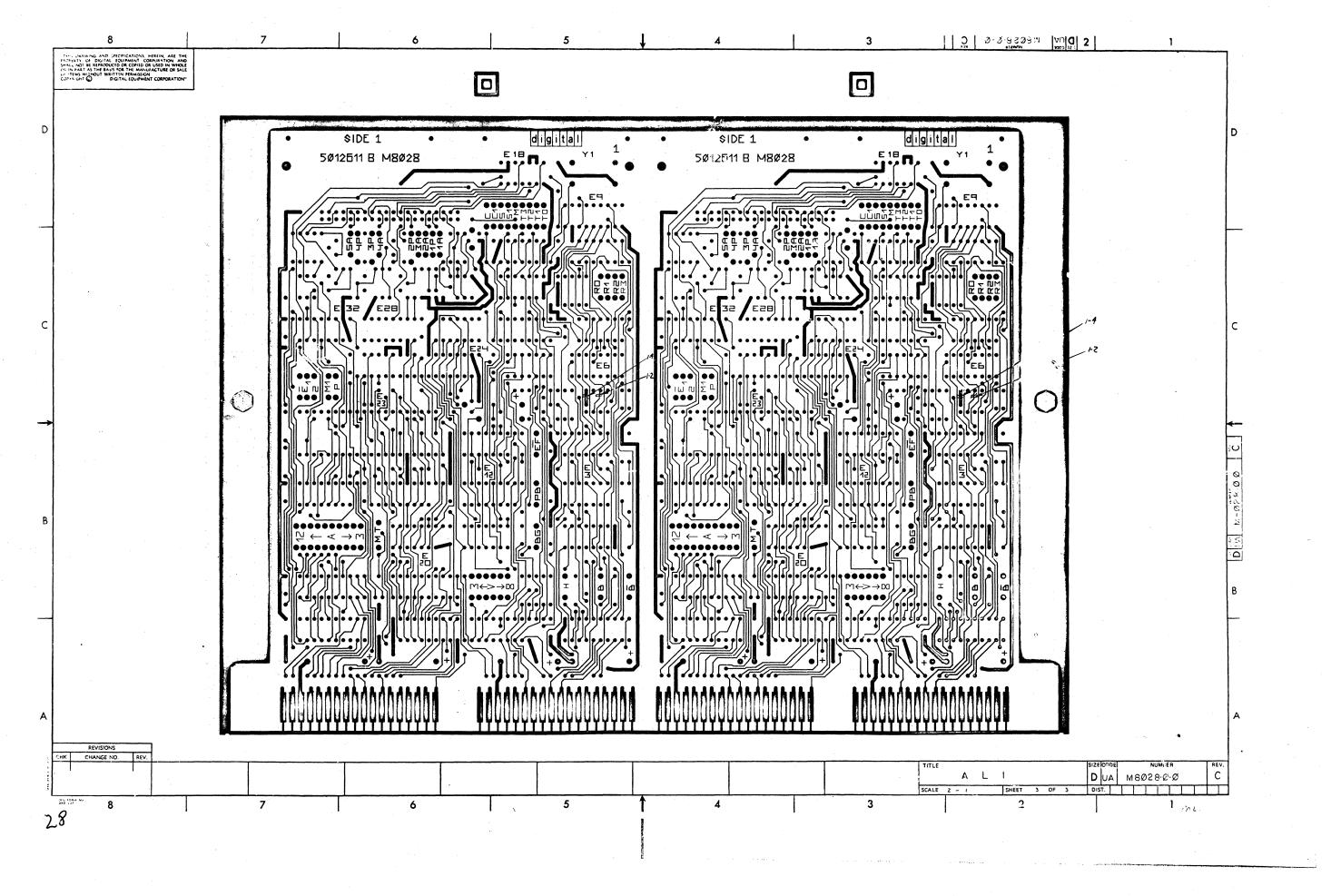


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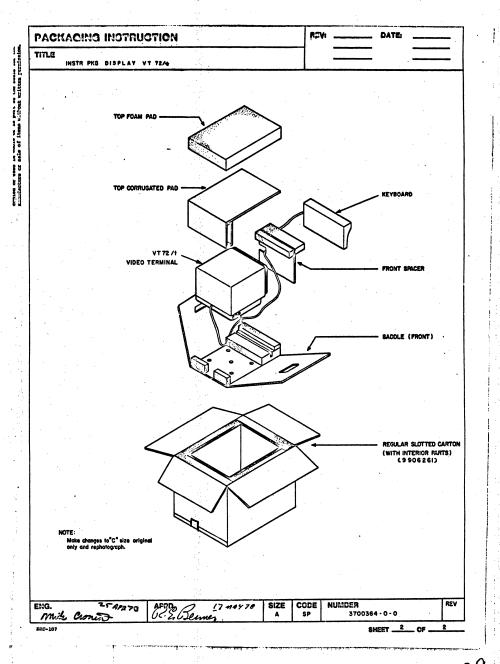


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PACK	aging instruct	TION	REV:	DATE:
TITLE	INSTRING DISPLAY	VT. 72/€		
		MATERIAL REQUIREMEN	13	
	Quantity	Purchase Specification No	Desc	ription
	1	9906261	Regular Slott	ed Carton (with
	7 ft	9905729	Carton Scalin	
		PACKAGING INSTRUCTION	NS	
Step		Procedure		
1.	Open Regular Slotted (corrugated saddle.	Carton (9906261). Remove top f	oam pad, top corrugated p	ad, front spacer and
2.	Place corrugated saddle	e on workbench.		
3.	Place VT72/t terminal	into saddle. Feet on terminal fit	into holes in saddle. (Fro	nt of terminal is
	positioned toward larg	er piece of foam.) nt spacer with feet placed into ho	ee (Spacer har faces away	(from foam)
4. 5.		keyboard into slot in foam on sad		, irom roum.
6.	· · · · · ·	up saddle and slide into foam-line		
7.	Route wires and cables	s behind terminal and along top co	urved portion of terminal	cover.
8.	Place top pad on top o	f terminal. (Foam block is positi	oned to the rear.)	
9.	Place top foam pad on	-		
10.	Close and seal Regular middle and one (1) str	Slotted Carton using one (1) strip across each end.	of carton sealing tape (99	05729) down the
				No. 1
				2. 2.

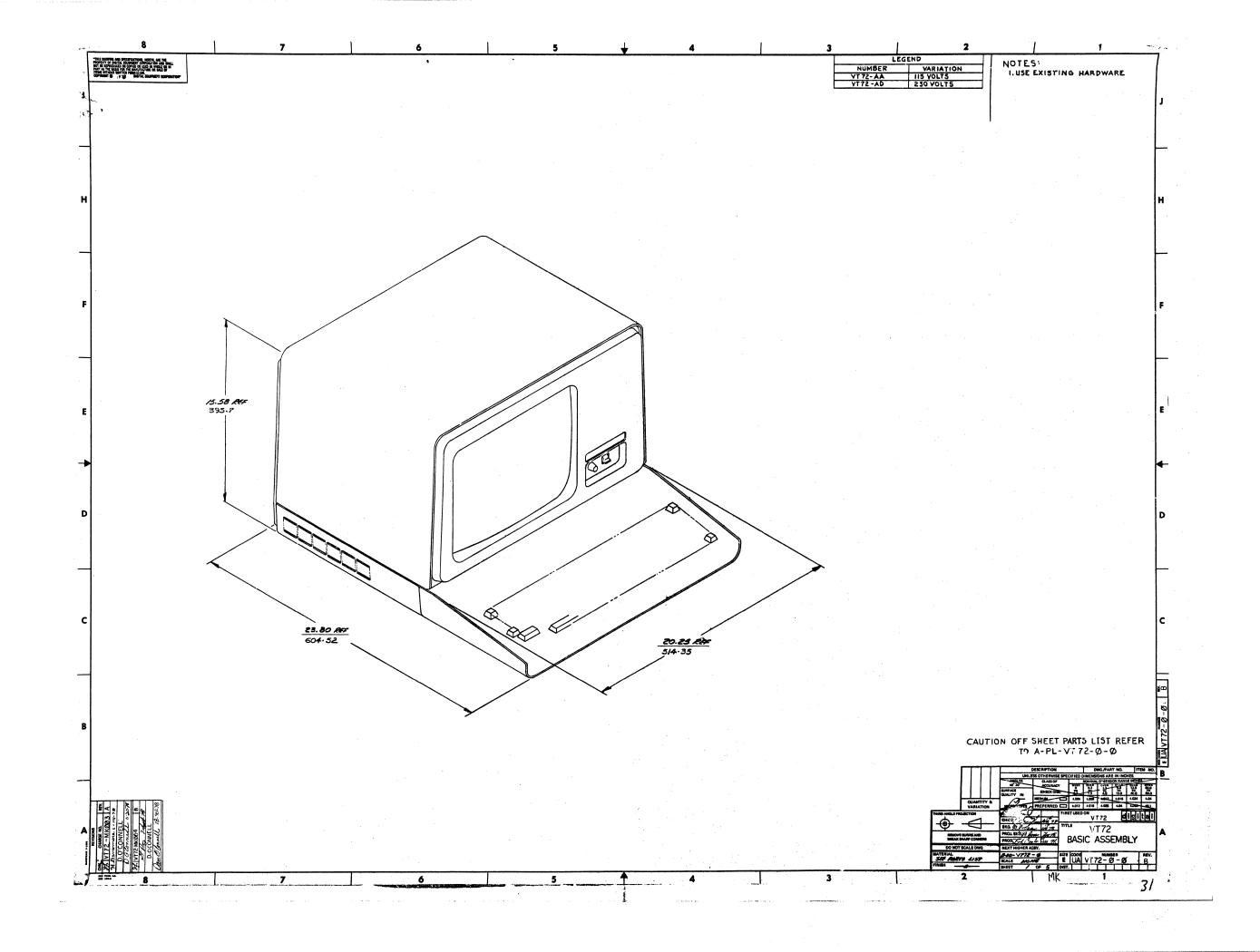


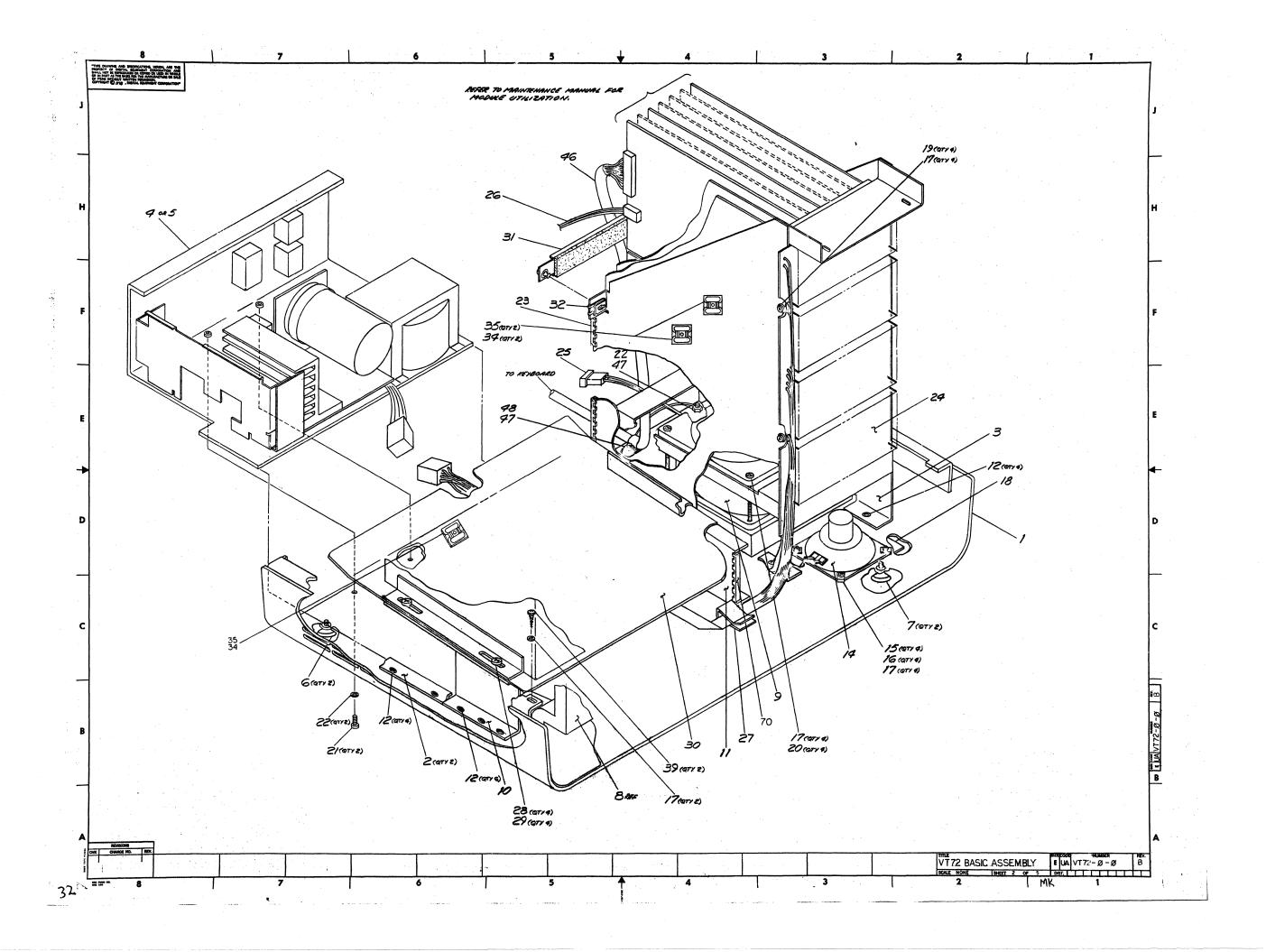
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FIELD MAINTENANCE PRINT SET

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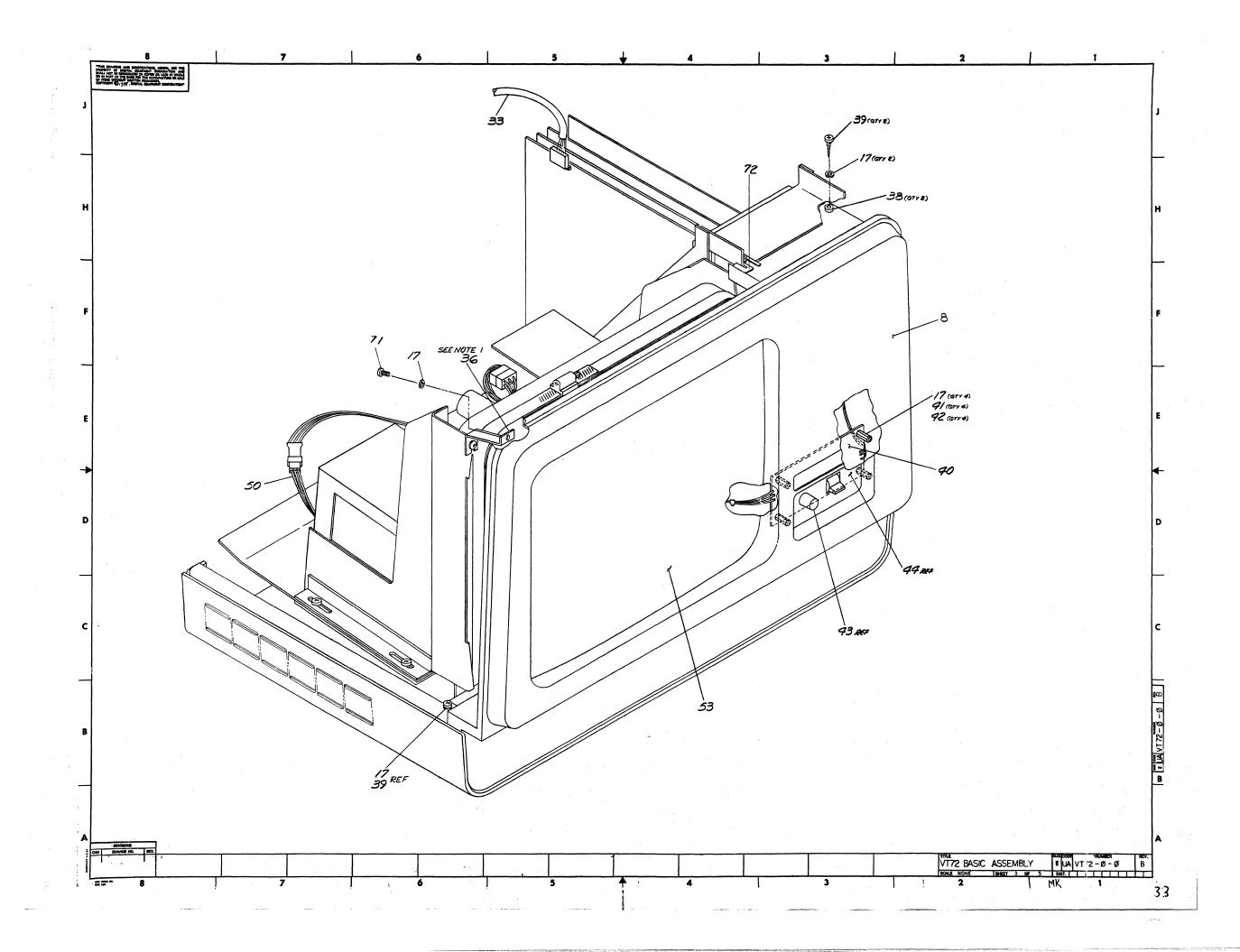
Table of Contents VT72 FIELD MAINTENANCE PRINT SET B-TC-VT72-Ø-7 C-IA-7012576-0-0 CABLE, VIDEO VT72 BASIC ASSY E-UA-VT72-Ø-ØACCEPTANCE PROC. A-SP-VT72-0-5 VT72 BASIC ASSY (PL) $A-PL-VT72-\emptyset-\emptyset$ PRODUCT SPEC. $A-SP-VT72-\emptyset-2$ B-MH-M8656-Ø-6 LKØ5 INTERFACE D-UA-M8656-Ø-Ø LKØ5 INTERFACE B-PL-M8656-Ø-Ø LKØ5 INTERFACE (PL) **UNIT VARIATIONS** D-CS-M8656-Ø-1 KYBD INTERFACE **COVERED BY THIS** A-SP-M8656-Ø-8 LKØ5 TO LSI-11 BUS INTERFACE PRINT SET VT71 CONTROL SECTION в-мн-м8657-уа-6 VT72-AA D-UA-M8657-YA-Ø VT71 CONTROL SECTION VT72-AD B-PL-M8657-YA-Ø VT71 CONTROL SECTION (PL) D-CS-M8657-YA-1 VT71 CONTROL SECTION A-SP-M8657-Ø-8 B-MH-M8658-YA-6 CONTROL MODULE VT71 VIDEO VT72/VOL 2 D-UA-M8658-YA-Ø VT71 VIDEO B-PL-M8658-YA-Ø VT71 VIDEO (PL) Field Maintenance D-CS-M8658-YA-1 VT71 VIDEO A-SP-M8658-Ø-8 VIDEO MODULE Print Sot VT71 BUS GRANT BOARD B-MH-M8659-Ø-6 D-UA-M8659-Ø-Ø VT71 BUS GRANT BOARD VT71 BUS GRANT BOARD (PL) B-PL-M8659-Ø-Ø VT71 BUS GRANT BOARD C-CS-M8659-Ø-1 P.S. UNIT ASSY E-UA-7015569-0-0 BOOTSWITCH & BRIGHTNESS CONTROL в-мн-5411990-0-6 D-UA-5411990-0-0 BOOTSWITCH & BRIGHTNESS CONTROL B-PL-5411990-0-0 BOOTSWITCH & BRIGHTNESS CONTROL (PL) BOOTSWITCH & BRIGHTNESS CONTROL D-CS-5411990-0-1 MODULE ECO HISTORY B-MH-5411776-0-6 H78Ø POWER SUPPLY D-CS-5411776-0-1 ASSY/DRILLING HOLE LAYOUT D-AH-5411776-0-5 PRINT SET ORDER NO. A-PL-KD11-HA PROCESSOR MP00613 в-мн-м7270-0-6 MODULE ECO HISTORY PROCESSOR D-CS-117270-0-1 E-IA-7015568-0-0 HARNESS, A.C. POWER D-IA-7015543-0-0 HARNESS, D.C. POWER TRANSFORMER ASSY D-IA-7015517-0-0 HARNESS, SPEAKER C-IA-7012279-0-0 CABLE, VT72 KEYBOARD D-IA-7014607-05 CABLE, BRIGHTNESS POT C-IA-7012446-0-0 D-AD-7014609-0-0 LOGIC ASSY VT72 BACKPLANE D-UA-7014605-0-0 DAN. DATE REV. digital USED ON OPTION/MODEL 6 APR 78 DBRIGHAM VT72 TITLE: VT72 FIELD MAINT. DATE 14 CHKD Bres PRINT SET AF2 78 PROJ. ENG. M. Goose 19278 CODE NUMBER SIZE REV. TC FIELD SERV. DATE B VT72-0-7 Cassal DIST. SHEET I OF ベルソフと DRB 124

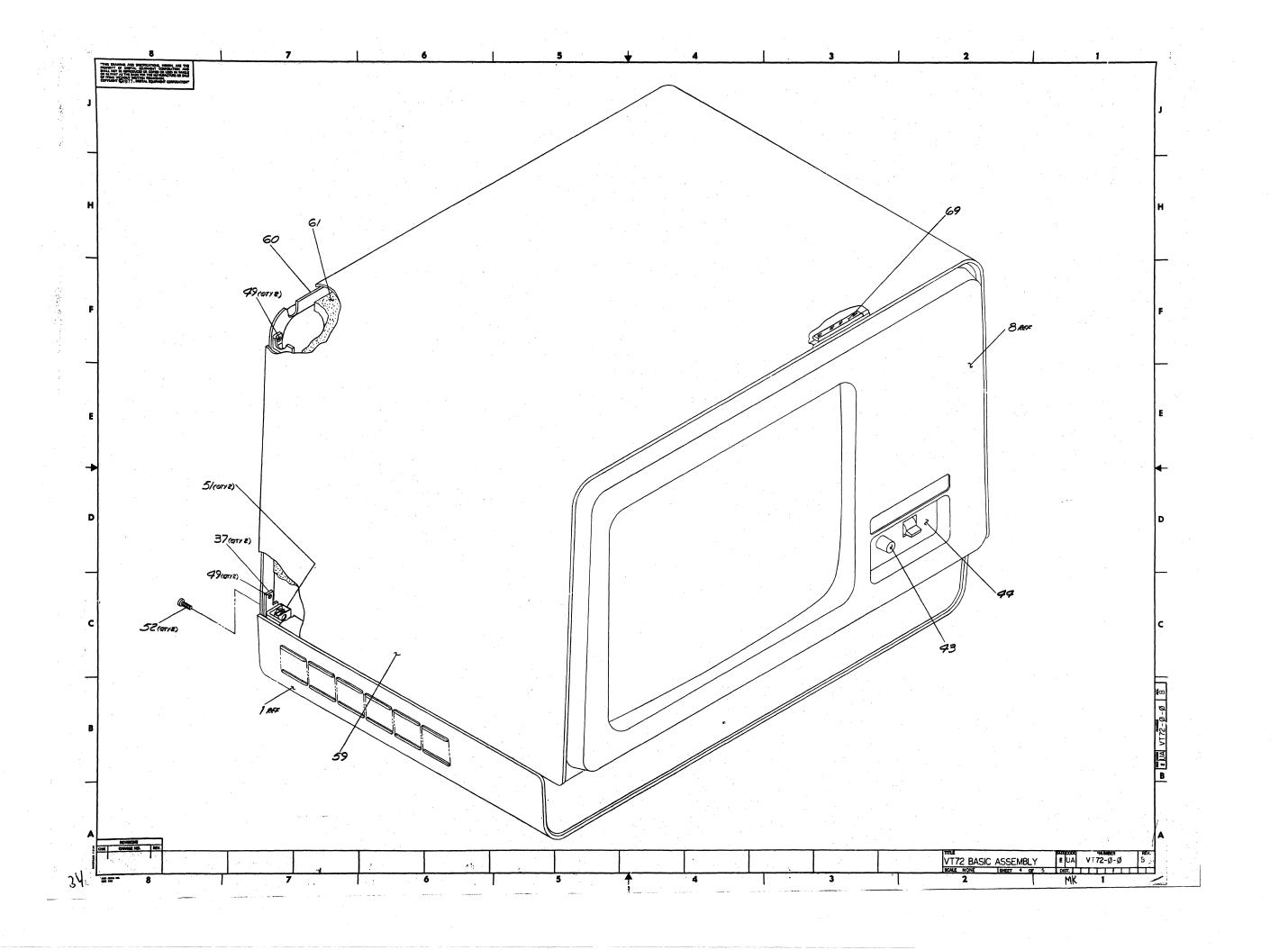


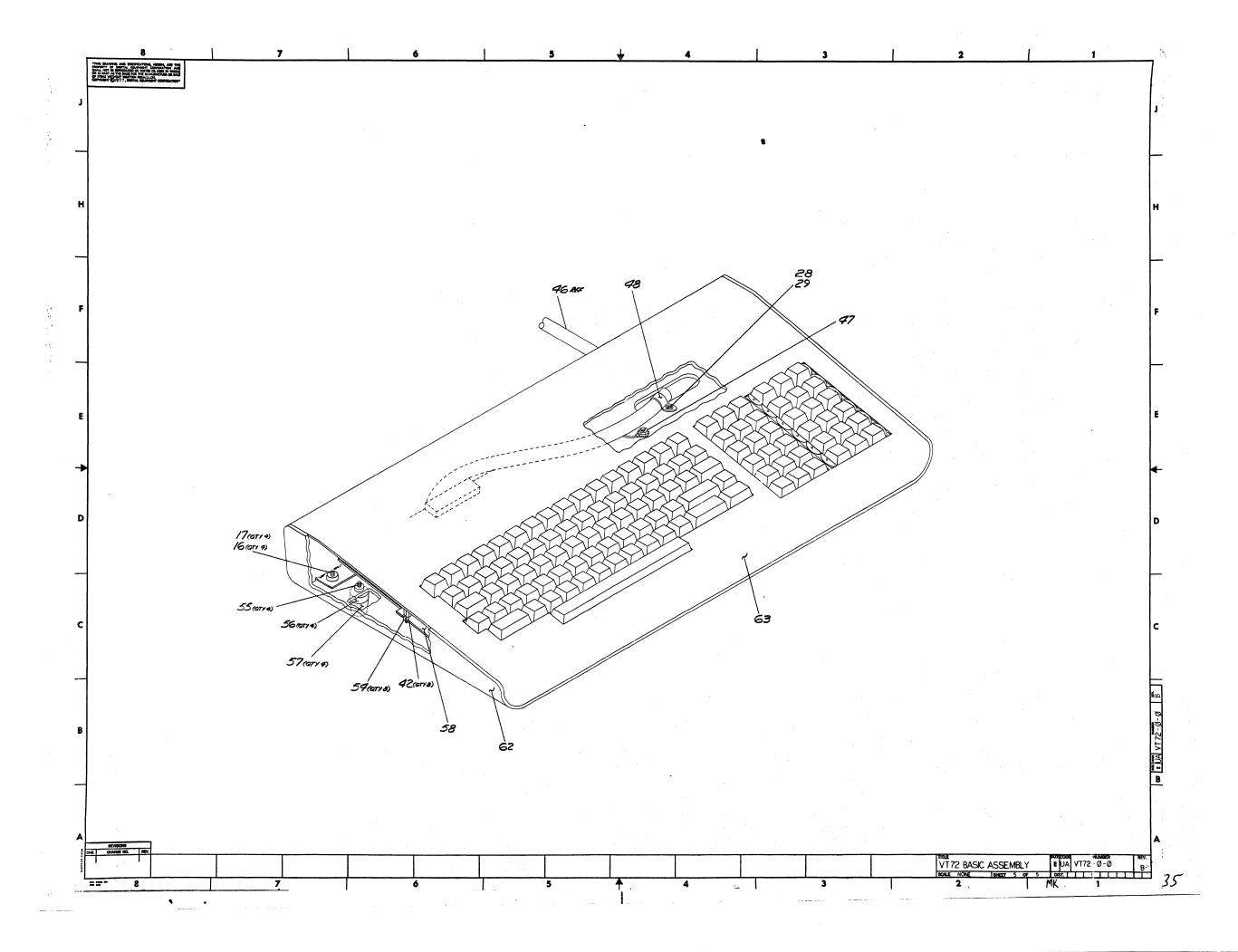


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1	D-IA-7014604-0-0	PAN ASSY, BOTT	ом			1	1						1	T	Т
2	B-MD-7420560-0-0	BRACKET, POWER	SUPPLY SUPP	ORT		2 .	2								
3	E-IA-7014125-0-0	CAGE, CARD				1	1				Τ.	T		T	
4	E-UA-7015569-00	POWER SUPPLY A	SSY (115V)		-	1	-						T		Π
5	E-UA-7015569-01	POWER SUPPLY A	SSY (23ØV)			_	1		П						
6	1214998-00	GLIDE, ADJ SWI	VEL .5 IN LG			2	2						\top		Π
7	1214998-01	GLIDE, ADJ SWI	VEL 1.5 IN LO	3		2	2						T	T	Γ
8	1215419	BEZEL, VT72				1	1					T	\top		
9	1213185-0-0	AIR MOVING DEV	ICE (70cFM			1	1						T	T	
.0	D-IA-7420032-0-0	BRACKET, MONIT	OR (L.H.)			1	1							T	
1	C-IA-7420604-0-0	BRACKET, MONIT	OR (R.H.)			1	1								
2	9000030-02	RIVET, DOMED H	EAD			18	18							T	
.3	C-IA-BCØ3T-25-Ø	CABLE, DLV11 T	OHOST	(NOT S	HOWN)	1	1					T	T.		
4	1210299-00	SPEAKER 2.5" P	ERM MAGNET			1	1		Г٦			T	Т	T	Γ
5	9008423-00	NUT-FLOATING C	LIP 6-32			4	4		П	T		T	\top	T	Γ
.6	9006023-01	SCR, PHL PAN H	D 6-32 X .44			8	8						\top	T	
7	9006633-00	WASH, INT TOOT	H DOCK #6			25	25								
.8	D-MD-7419542-0-0	SCREEN				1	1							Τ	
9	9006021-01	SCR, PHL PAN H	D 6-32 X .31			4	4								
20	9006031-01	SCR, PHL PAN H	D 6-32 X 1.7	5		4	4						\bot		
1	9006039-01	SCR, PHL PAN H	D 8-32 X .50			2	2					$\perp \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \! \!$			
22	9006634-00	WASHER, INT TO	OTH LOCK #8			3	3								
ITLI	VT72 BASIC ASSE	EMBLY	ASSY NO. E-UA-VT	72-Ø-Ø	A	PL		VT	NUMB 2-Ø-				REV C	ECO MK	
	223 11001		SHEET 1 O	F 4	DIS	г		1	T	T		Т		T	1

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NO.	DWG NO./PART NO.		DESCRIPTION			5	5						- 1	
23	9007035-00	GROMMET CATERP	ILLAR			A/R	A/R						\Box	
24	D-AD-7014609-0-0	VT72 BACKPLANE	ASSY			1	1							
25	C-IA-7015555-0-0	FAN LOGIC CABL	E			1	1						\perp	
26	C-IA-7012279-0-0	HARNESS, SPEAK	er î			1	1							
27	9009636-00	CLAMP, CABLE A	DHESIVE BACK	ζ		1	1							
28	9006071-03	SCR, PHL TRUSS	HD-10-32 X	.38		5	5							
29	9006636-00	WASH INTO TOOT	H LOCK #10			6	6							
30	D-MD-7419539-0-0	SHIELD MAGNETI	С			1	1							
31	C-MD-7014129-0-0	RETAINER ASSY	P.C. CARD			1	1	T					\Box	
32	9008196-00	⅓ TURN RECEPTA	CLE			1	1							
33	C-IA-7012576-1L	CABLE VIDEO				1	1							
34	9008264-00	CABLE MOUNT AD	HESIVE			3	3.							\Box
35	9007031-00	CABLE TIE				3	3							
36	B-MD-7419846-0-0	BRACKET, BEZEL				1	1	T	П		7-			\Box
37	B-MD-7420894-0-0	STATIC BAND				2	2	T	П		T		\top	
38	9009283-00	SPACER HEX #6	x .125			2	2	T			1		Т	
39		SCR, PHL PAN H	D SHEET META	AL #6 X .75		4	4		П				T	
40	D-UA-5411990-01	BOOT SWITCH &	BRIGHTNESS (CONTROL		1	1							
41	9006026-01	SCR. PHL PAN H	D 6-32 X .7	5		4	4							
42	9008120-00	SPACER HEX #6	x .44			12	12							
43	1213274-01	KNOB BRIGHTNES	s			1	1						\Box	
44	B-IA-7420033-0-0	LOGO BRIGHTNES	s			1	1							
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NO.	DWG NO./PART NO.		DESCRIPTION		VII.	VII.7								
45	3613210-	TAG SERIAL			1	1		T						
46	D-IA-7014607-05	CABLE VT72 KEY	BOARD		1	1								Ĺ
47	9006563-00	NUT KEPS 8-32			3	3					\perp	⊥.		Ĺ
48	9007086-00	CLAMP, CABLE			2	2								Ĺ
49°	9000030-05	RIVET DOMED HE	AD		4	4								Ĺ
50	C-IA-7012446-ØM	CABLE BRIGHTNE	SS		1	1								L
51	9007786-00	NUT SPEED, 10-	-32		2	2								
52	9000039208	SCR, F.H. 10-3	32 X .50 LG. (BLACK)		2	^2								Ĺ
53	3012537-01	DISPLAY RASTE	R MODULE		1	1		T	П					Ĺ
54	9008185-00	NUT KEPS 6-32			8	8		T			T	T		Ī
55	900607 5 -01	SCR, PHL PAN I	ID 10-32 X .75 LG.		4	4		T	П					Ī
56	B-MD-7415829-0-0	SPACER			4	4		T			T			ſ
57	9009267-00	BUMPER			4	4								Γ
58	3012538-01	KEYBOARD LKØ5-	-A 112 KEYS/12 LED		1	1		T			T			Ī
59	D-IA-7014603-0-0	COVER ASSY			1	1		T						Ī
60	1215420	COVER REAR			1	1		T			Т			Ī
61	C-MD-7416633-01-0	FOAM (COVER AS	SSY)		1	1		T			Т	T	П	Ī
62	E-IA-7419534-9-0	BASE, KEYBOARI)		1	1					T		П	Ī
63	E-IA-7419533-Ø-Ø	COVER, KEYBOAR	SD .		1	1					I			Ĺ
64	D-UA-M8659-Ø-Ø	GRANT BOARD			1	1								Ĺ
65	A-PL-KD11-HA-0	KD11MA PROCESS	SOR		1	1	Т	Π	Π		T			Ĺ
66	D-UA-M8658-YA-Ø	VT71 VIDEO MOD	ULE		1	1								Ĺ
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57	D-UA-M8657-YA-Ø	VT71 CONTROL	SECTION		1	1							
8	D-UA-M8656-Ø-Ø	LKØ5 INTERFAC	E		1	1		\bot		\sqcup	\dashv		\perp
59	B-MD -7421669-0-0	FOAM, BEZEL			1	1	$\sqcup \bot$	4	\bot	\perp	\dashv		丄
70	9007036 - 0 0	GROMMET, CAT			M∕R	^∕ _R	\sqcup	4		$\perp \perp$		\perp	1
71	9006028-01	SCR PHL PAN	HD 6.32X1.0			1	$\sqcup \bot$	1					\perp
72	C-MD-7421401-0-0	BRACKET, CARL	CAGE		1	1	\perp	4	1_	$\sqcup \bot$	$\dashv \dashv$		4
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TITLE VT72 HARDWARE SPECIFICATIONS VT72 User Specifications Summary - 15" Alphanumeric Display - 24 Rows of Characters - 80 Characters per Row - 256 Code Extended Character Set - 4 Special Display Modes - Blink - Bold - Underline - Half Reverse Video - DEC Standard Main Keyboard - 36 System Defined Function Keys 16 User Definable Function Keys Indicator Lights - On/Line or Off/Line Operation - Programmable Character Set SIZE CODE

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VT72 HARDWARE SPECIFICATIONS

Section 0 - OVERALL DESCRIPTION

The VT72 is an LSI-ll based upper/lower case intelligent terminal $\,$ programmed to perform complex editing tasks by interaction between the user, the keyboard and a raster scan display.

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Most of the features of this terminal will be defined by software. These features will be listed in the section under "OVERALL EDITING FEATURES", but will only describe the hardware necessary to interact with the software to make an editing terminal. ${\tt A}$ separate document will describe the software and detailed features of the VT72 as an editing terminal.

The VT72 is a table-top unit with monitor, keyboard, power supply, logic, fans, etc., in the one enclosure. Quad or half-quad modules plug into a double system unit wired assembly. There is room in the wired assembly for expansion to 28K of memory and/or expansion of other Q bus controllers. See the appendix for the layout of the wired assembly.

As shown in the block diagram in the appendix, the VT72 is a standard LSI-11 with the addition of two special modules to drive the display, and one special module to read the keyboard and drive the keyboard lights. All other modules are standard LSI-11 modules.

The basic VT72 does not contain mass storage although room for expansion of the Q bus to include a floppy disk control is available in the basic VT72. The VT72 without mass storage is loaded from a host computer via the DLV11-F serial asynchronous line interface module.

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Section 1 - SPECIFICATIONS

1.0 General

These are the general specifications of the hardware but do point out features possible when software is added. If the feature is performed by software, this fact is noted in the feature description.

- 1.0.1 The displayable screen area is 240 horizontal sweep lines, each line made up of 800 dot positions. A character is made up of a 10 X 10 dot matrix. The screen is therefore made up of 24 character rows, and each row contains 80 characters.
- 1.0.2 Individual characters can be displayed in normal, reverse video, bold and underline modes. These modes are additive, ie., bold reverse video. Under program control, individual characters can also be made to blink. They can be made halfintensity by displaying the character on alternate sweeps. The only limitation to character display modes is that there should not be more than $20\,$ changes in display mode per character row. For example, 10 non-contiguous reverse video (or bold or blink or underline) blocks of characters can be displayed in the same row as 10 non-contiguous blocks of characters. If the limitation is exceeded, the screen will flicker.

An alternate method of programming is available for applications that require extensive character mode changes. The programmable character set of 256 characters can be used to describe characters of different display modes. For example, the first 128 characters could be normal while the second 128 characters could be the same characters except in reverse video.

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LE VT72 HARDWARE SPECIFICATIONS

1.1 Display Monitor

The monitor is a standard 15 inch CRT. There are 80 characters per row, 24 rows; normal, blink, bold, underline and half-intensity reverse video. Half-intensity by software of normal, underline, and half-intensity reverse video is possible by turning off selected portions of the display on alternate sweeps. Blink rate is controlled by the software.

1.2 Keyboard (LK05 Var. -01)

The sculptured keyboard has N key rollover and uses Hall effect devices.

The parallel keyboard produces unique codes for each key. The main keyboard is a DEC standard keyboard with the addition of 16 keys above the normal top row of keys.

There are two function pads, each containing 18 keys. The right most function pad has 6 lights down each side of the pad. The distance between the two pads is ½ a key width so 1.5 wide key caps can be used to fill the space between the two pads. In this case, the left most lights must be removed.

1.2.1 Unique Features

Some function pad keys produce one code when depressed and another code when released. This allows the software to carry out a function at an arbitrary speed which is pleasing to the human operator (ie., scroll) but start and stop this function when the operator interacts with the key. These keys are: the last 3 rows of the left function pad, the last 2 rows of the right function pad, one key in the upper left corner of the right function pad, and the repeat key on the main keyboard.

1.2.2 Keycaps

This whole keyboard can be depopulated to tailor the keyboard to a particular application. In addition, all keycaps are removeable; keycaps can be ordered with clear plastic tops with a user-changeable insert for legend.

See the LK05 purchase specifications for more information on this keyboard. PS-30-12538, var. -01.

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If EOT is detected, the display controller stops access from memory until the whole display cycle is repeated. $\,$

If the number of characters specified in the parameter word have been read from memory by the display control, the display control will pick up another parameter word and text pointer. It will read the contents of the wired address, increment it by two and write the incremented information back into the memory. This incremented information will then be used as the address of the second text address/parameter word/text pointer pairs. The cycle then continues as before.

There can be a large number of parameter word and text pointer pairs to define BLOCKS OF TEXT. A block of text can be as large as 2048 characters or as small as 1 character. For example, the cursor is usually defined as a one character block. Each contiguous piece of text not in the same display mode must be a separate block. For example, if 3 words were displayed, the first word normal video, the middle word reverse video and the last word normal video, three blocks would define this video presentation. Text, of course, can be contiguous in memory or scattered in blocks throughout memory.

1.4 Character Generator

The character generator is capable of displaying 256 unique character codes. The character generator is loaded under program control when the terminal is first initialized. This means that changing characters does not involve hardware changes, only changes to a list in memory. This feature is known as a "programmable character set".

Characters are displayed in a 10 X 10 dot matrix. The whole screen is comprised of contiguous 10 X 10 dots squares, 80 to a line, in 24 lines, a total of 800 horizontal, 240 vertical dots. Because spaces must be left between characters and between lines, the actual character is usually displayed in a 8 X 8 matrix. The 9th horizontal scan line in the 10 X 10 matrix is underline. The 10th horizontal scan line is usually left blank as a space between character lines. The VT72 character layout is shown in the appendix. Computer convention shows numbering from 0 to 9 instead of 1 to 10.

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1.3 Interface to LSI-11

Text packed 2 characters to a 16 bit word is taken directly from memory (DMA) into the display controller. The controller has two shift registers that can store 80 characters each. One shift register drives the display while the other is loaded from memory. After a row of characters has been displayed, the functions of the two shift registers are reversed.

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The method of accessing text in memory is similar to the 3-cycle data break of the PDP-8. In the VT72, a wired address contains a pointer of address to a list of parameter words and text address. This list is called a DISPLAY TABLE. A 16 bit parameter word and a 16 bit text address define a block of text to be displayed on the screen. These two words are in consecutive memory locations.

The PARAMETER WORD is a 16 bit word. The least significant 11 bits of the parameter word are the number of characters to be displayed. Another 4 bits in this 16 bit word define whether the text is to be blank, bold, underline or reverse video. The most significant bit (if a one) connects the parameter word to a JUMP instruction so that the contents of the next memory location are jammed into the word address. This feature and the bit assignment of these two 16 bit words is detailed in the section on programming.

The 16 bit text address word, also called a TEXT POINTER, is the current address of the text being loaded into the display controller shift register.

DISPLAY SEQUENCE - The display control reads text for the first character row while a blank row above the normal screen area is being displayed. The display control first reads the contents of the wired address (INITIAL DISPLAY TABLE POINTER) and uses it as an address to read the first parameter word and the associated text pointer word into hardware registers in the display control. The parameter word is used to determine the display mode and to count the number of text characters to be taken from memory. The display control used the text pointer to address memory, increments the hardware register containing this address and used hardware to count the number of characters read from memory equals the number of characters that were previously read from the least significant 11 bits of the parameter word.

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The 10 horizontal and 10 vertical dots which define a character are generated by 10 "words", each 10 bits long. There is one 10 bit word for each of 10 horizontal scan lines which make up a character. Each 10 bit word therefore defines one horizontal scan line of a character.

The character generator is loaded from memory by the display controller. This information contains 20 words for each ASC11 character plus the ASC11 character. These words are 16 bits

The software starts this loading sequence by setting Bit 15 of the Command and Status register. When the display controller is finished displaying the current frame, it then reads the contents of a jumper selectable address, the character list pointer. The contents of this address is the starting address of a table containing the character generator information. These contents are read into a register that can be incremented and used by the display controller as an address to do DMA's from memory to the character generator RAM.

It is possible to change 1 or 256 characters in the character generator since the software has control of memory contents and therefore the starting address of the table, the length of the table and the data describing the displayed character to be associated with each ASC11 code. Details of loading the character generator is contained in the programming section.

1.5 Panned Scrolling

The software of the LSI-ll can interact with the display hardware so scrolling occurs smoothly instead of jumping one character row at a time. When scrolling is requested from the keyboard, the software preloads a counter in the display control with a number that can vary from 6 to 17. This number represents the fraction of a character row the display will scroll, from 1/10 to 9/10 of a character row.

When scrolling text up, the top scan line disappears from the screen and a new scan line appears at the bottom of the screen. Software changes the text list pointers so 25 rows of characters instead of 24 rows of characters are displayed on the screen. Since there is only room on the screen for 24 complete rows, part of the first and last row will be missing. The offset number determines how much will be missing. If this number is 7,

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10% of the top row and 90% of the bottom row will be missing. The software changes this number at a regular rate, which is some multiple of the display frame rate (60 HZ or 50 HZ). When the number reaches 17, 90% of the top row and 10% of the bottom row will be missing. The next time the software changes this number, the number will be changed to 6. At the same time, the text list pointer will be changed so only 24 rows of characters are displayed, the top row will have disappeared completely from the screen and the bottom row will be completely on the

Scrolling downwards is similar.

1.6 Unique Codes

The display hardware detects 8 unique codes: ASCII code -

> 00 & 200 END OF TEXT 01 & 201 END OF LINE 03 & 203 END OF LINE

When an END OF LINE code is detected by the hardware, DMA from $\,$ memory for that line is stopped and the rest of the shift register is loaded with the space code to effect a blank of the display line after the END OF LINE code.

When END OF TEXT code is detected, DMA from memory is stopped for the remainder of that display cycle and the screen is blanked from the END OF TEXT code to the bottom of the screen. Eight codes are provided so as to allow displayable and non displayable line terminators.

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16K MSV11-DC MOS Mem

1	Not Used	Not Used	2
4	11 11	11 11	3
5	n n	" "	6
8		. и и	7
9	LSI-11	*MRV11-VC	10
12	MSV11-DC (16K)	Grant Board	11
13	DLV11-F (Ser)	Keybd Control	14
15	Display	Control	
	Video	Control	

28K using MSV11-DC MOS Mem

1	Grant Board	Not Used	2
4	Not Used	e	3
5	и и ,	11 11	6
8		6 17	7
9	LSI-11	*MRV11-VC	10
12	MSV11-DC (16K)	MSV11-DC (16K)	11
13	DLV11-F (Ser)	Keybd Control	14
L3 L5	Display	Control	
	Video	Control	

16K MSV11-CD

1	Grant Board	Not Used	2
4	Not Used	11 11	3
5	11 11	11 11	6
8	и п	11 11	7
9	LSI-11	*MRV11VC	10
12	MSV11	-CD	11
13	DLV11-F (Ser)	Keybd Control	14
15	Display	Control	
	Video	Control	

28K Using MSV11-CD MOS Mem

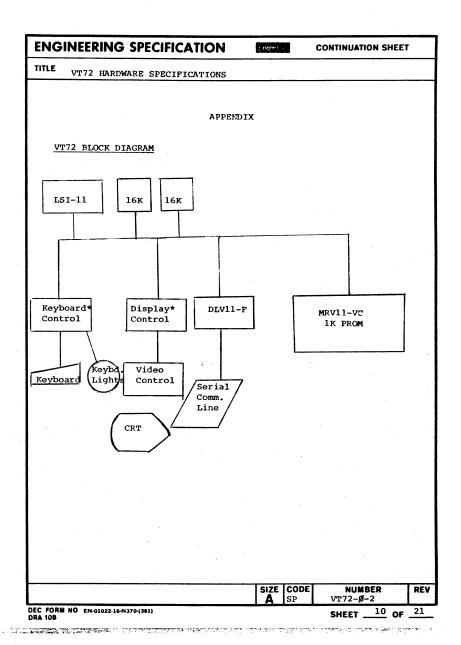
1	Grant Board	Not Used	2
4	Not Used	" "	3
5	H H	0 11	6
8	LSI-11	*MRV11-VC	7
9	MSV11-	CD (16K)	10
12	MSV11-	CD (16K)	11
13	DLV11-F (Ser)	Keybd Control	14.
15	Display	Control	
	Video	Control	

Note: If no MRV11-VC in Conf. substitute grant board in slot.

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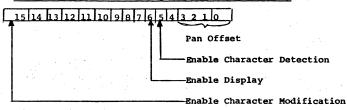
2.0 Display Processor

The VT72 Display Processor consists of a M2657-YA and M8658-YAmodule. It is a microcontrolled device with DMA control over the LSI-11 bus. As such its operation is separate from the LSI-11 once its parameters have been set-up. The display will continue even if the LSI-11 has halted program execution. The VT72 has a writable character store which also operates as a DNA function. The character set is totally in volatile memory and must be rewritten at every power-up time. In addition, the display has the ability to smooth scroll (pan) and detect end of line (EOL) and end of screen (EOS).

The display processor generates a raster scanned video presentation composed of 240 scan lines made up of 800 dot positions. A character is made up of a 10 X 10 dot matrix. The raster is therefore made up of 24 character rows each containing 80 characters. See Purchase Spec. 30-12537 for a timing diagram of the video information.

3.0 Programming

3.1 VT72 Command And Status Register 177670 (Standard)



It is very important to remember that register is not a hardware register. It is a window into the microcontroller. The controller will only look at these bits at the correct time in relationship to raster on the screen. However, this does allow the unique ability of being able to redefine any single character while displaying. The microcontroller will use the vertical fly-back time to do this, and the screen will never flicker. The programming concepts will be discussed later. However, the

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individual bits will be identified now.

3.1.1 Pan Offset: Bits 3-0

This is a write only register which gives the display the capability of smooth scrolling. The register has a legal value range from 6 to 17. The value of 6 is the normal pan offset. The pan bits must always have \underline{some} value whenever the register is loaded. Each increment of the pan register offsets the screen by one scan:

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Scan Line	Pan Offse
0	- 6
1	7
2	10
3	11
4	12
5	13
6	14
7	15
8	16
9 .	17

Ex: When the pan register equals 10, 8 scans of Row \emptyset are displayed, 10 scans of Rows 1-23 and 2 scans of Row 24. It is important to note that although only 24 rows of text are displayed on the screen 25 rows are always loaded by the micro controller. To scroll up start the pan register at 6 and increment to 17 - to scroll down start at 17 and decrement to 6.

When scrolling the pan register may only be changed once per vsync (discussed later) and must be changed not less than once every other vsync or the screen will flicker. However, it may be incremented in an accelerating manner to as much as a whole row per vsync and still look smooth.

Enable Character Detection: (Bit 5)

This bit enables the action of the special characters for END OF LINE and END OF SCREEN. When bit 5 is a zero, these characters are treated as any other characters.

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C. Both the Enable Display and the Enable Character Modification bits may not be set if the micro is not already displaying. This is due to the fact that the micro-controller may see the Enable Display bit before the Enable Character Modification bit and destroy the contents of the CLP. (See preceding Section $\ensuremath{\mathtt{B}}\xspace)$. Correct sequence of operation would be as follows:

- I. Set up IDTP (Section 3.2.4) to point to EOS (Section 3.1.2) character.
- Turn on display (screen should be blank because EOS has not been defined).
- Wait 1/60 of a second. (Be sure bit has been seen).
- Write the character set and read display on (MOV #100146, @ #177670).
- V. The micro-controller is ready to display.
- If the micro controller is displaying:
 - A. The last loaded address will be returned to the CLP and won't change because the display is already on.
 - Only one character may be written at a time or the display may flicker.
 - If, however, it is desirable to write the entire character set as long as the last 2 lines of text are blank the display will go blank for the write

NUMBER √<u>T72</u>-Ø-2

ENGINEERING SPECIFICATION

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VT72 SPECIFICATIONS

ASCII Character 0 & 200 END OF TEXT 1 & 201 END OF LINE 2 & 202 END OF LINE 3 & 203 END OF LINE

These codes are detected by hardware but since the character generator is programmable, the codes will be displayed.

3.1.3 Enable Display Bit 6

This is a write only bit that when set enables the terminal to display. While displaying the microcontroller will give an interrupt every vsync time. Vsync is defined to be the time just after the microcontroller has loaded from the pan register and after it has picked up the initial address of the display list from the IDTP (Initial Display Table Pointer). At this point either of these values may be changed.

3.1.4 Enable Character Modification: Bit 15

This bit when set will initiate the writing of characters at an address pointed to by CLP (Character List Pointer). Whenever this bit is set the pan value <u>must</u> be set to 6 or the characters will be offset. The enable display and enable character detection bits may be on at this time. However, only one character may be written without screen flicker.

The list is terminated by a zero in the low order byte. When the micro controller is done loading, the terminating address will be deposited in the CLP. It is important to note that several precautions are necessary here.

- 1. If the micro controller is not displaying:
 - A. A random pattern of lines and characters will be displayed while writing. Finally before the display is enabled a strange pattern may be left on the screen.
 - B. While the CLP will contain the last loaded address after writing the CLP will contain a random address once the enable bit is turned on.

DEC FORM NO EN-01022-16-N370-(381)

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ENGINEERING SPECIFICATION

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VT72 SPECIFICATIONS

3.2 Hardware Vectors (Pointers)

	<u>VT/1</u>	
XX0	360	PC Wector Pair
XX2	362	PSW
XX4	364	CLP - Character List Pointer
XX6	366	DTP - Display Table Pointer
XX10	370	IDTP - Initial Display Table Points

3.2.1 Vector Pair:

Standard PDP11 interrupt v ctor pair micro controller interrupts here every vsync time.

3.2.2 Character List Pointer:

Should contain the first address of the character list before the enable character modification bit is set. The location may be used to determine when the micro controller is done since it returns the last loaded address to the CLP when done.

3.2.3 Display Table Pointer:

correct Display Table Address. Whenever the current display table's byte count overflows the micro controller goes to the next display adder by incrementing the address in this position by 4.

3.2.4 Initial Display Table Pointer:

The micro controller loads the DTP from this address just prior to vsync time.

3.3 Text Format 15

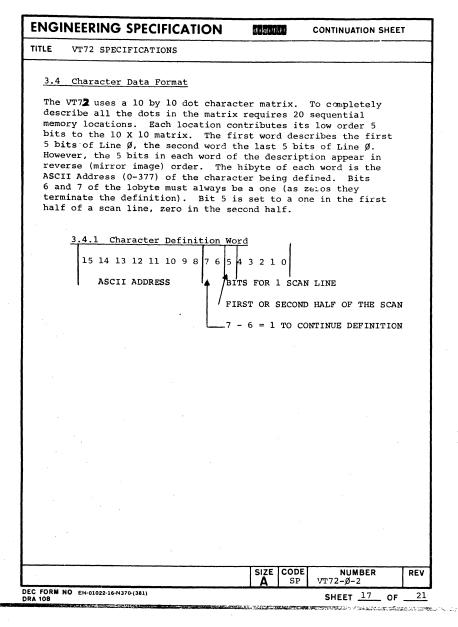
HIGH BYTE LOW BYTE

Text can start or stop on a high byte or low byte. The full 8 bits are decoded to form a character. The appendix lists the standard 256 characters.

SIZE CODE

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DEC FORM NO EN-01022-16-N370-(381) DRA 108



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TITLE '	VT72	SPE	CIFIC	CATIONS												
122 123 124	12Ø 121	118 119	116 117	112 113 114 115	10/8 10/9 11/0 111	1 <i>0</i> 6 1 <i>0</i> 7	104	103	101	1,00	98	96 97	95	94	91 92	90
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	111111111111	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	111	CHARACTER AND "-" CORRESPONDS TO A BLANK CHARACTER, OPTIONALLY, EROES MAY APPEAR ANYWHERE WITHIN THE DISPLAY. THEY ARE NOT SHOWN.	; ; FINALLY THE EXPANDED REPRESENTATION OF "3". EACH CHARACTER ; REPRESENTS A BYTE IN THE DISPLAY, X CORRESPONDS TO A NON-BLANK			gallagillil	$\mathcal{G}(x)$	ggliggillli . x ggliggillig . x	$: ggllgglllll \dots ggllggllllg \dots x \dots ggllggllllg \dots x \dots x$; ggilggilll	× · · ·	;	; UPPER 11 BITS ARE SEPARATED FROM THE LOWER 5 BITS FOR LEGIBILITY. ; ALSO .'S REPLACE 0'S AND X'S REPLACE 1'S IN THE LOW ORDER BITS.	; BELOW IS AN EXAMPLE OF THE CHARACTER "3". ; THE ARRAY IS DRAWN AS 2 WORDS BY 10 WORDS, IN EACH WORD, THE
							SIZ		COD SP	E		NU 2-Ø	MBI	ER		REV

ENGINEER	ING SPECIFICAT	ION) rigin't		CONTINUATION SHEET	 Г
TITI F	SPECIFICATIONS					
V172 .	PECIFICATIONS					
THE CHARAC	CTER DEFINITION WO	RD FORMAT				
Word	Raster Scan	Bit 5		i	Bit 5 = Ø	
mor a	Raster Stan	First	наг		Second Half	-
1	Scan Ø	х				
2	Scan Ø				x	
3	Scan 1	x				
4	Scan 1				x	
5	Scan 2	Ţ			•	
6	1	х				
	Scan 2				х	
7	Scan 3			ĺ	X	
8	Scan 3				x	
9	Scan 4	х				
10	Scan 4				x ,	
11	Scan 5	х				
12	Scan 5				x	
13	Scan 6	· x				
14	Scan 6				· x	
15	Scan 7	x		Ì		
16	Scan 7			l		
					x	
17	Scan 8	х				
18	Scan 8			-	x	
19	Scan 9	x				
20	Scan 9		CIZE	CODE	X	DEV.
			A	SP	NUMBER VT72-Ø-2	REV

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE VT72 SPECIFICATIONS

CONTINUATION SHEET

SHEET 18 OF

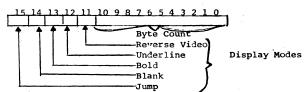
21

3.5 Display Table

DEC FORM NO EN-01022-16-N370-(381) DRA 108

The display table consists of one or more entries (Display Blocks) each containing two elements. The parameter word which contains the display information and the byte count. Secondly the byte address where the display list begins. The maximum total display blocks per line is 20.

3.5.1 Parameter Word



3.5.2 Byte Count:

Two's complement of the desired number of bytes to be displayed using this parameter word. Once the byte value has overflowed the microcontroller will continue on to the next sequential parameter word and address pair. The byte counts overflows at 3777 rather than Ø due to certain hardware constraints. If BC = 3777 is loaded the micro processor will go immediately to the next display block.

3.5.3 JUMP:

The JUMP is a command to the microcontroller when bit 15 is set the rest of the parameters word is ignored and the address that follows is jam loaded into the DTP. This address is the start of the new display list. Care must be taken in using JUMPS. As a general rule of thumb one JUMP has the same overhead as one display block. (ie., 1 JUMP + 19 BLOCKS = 20 Display Units).

ENGINEERING SPECIFICATION

digital

CONTINUATION SHEET

TITLE VT72 SPECIFICATIONS

NOTE: When the display processor is heavily used 14-20 display units per line 30-45% of all processor time will be devoted to DMA accessory for display.

3.5.4 Display Modes

These modes are tied to the particular block. The mode will continue through the block until the byte count overflows. Then the next modes are loaded with the new byte count. The microcontroller treats the blank bit the same as the others so the display list for that block must be valid (not EOL or EOS characters unless desired).

3.5.5 Reverse Video:

Reverses the intensification of the character matrix.

3.5.6 Underline:

Turns on the 9th scan line.

3.5.7 Bold:

Intensified by two the character matrix.

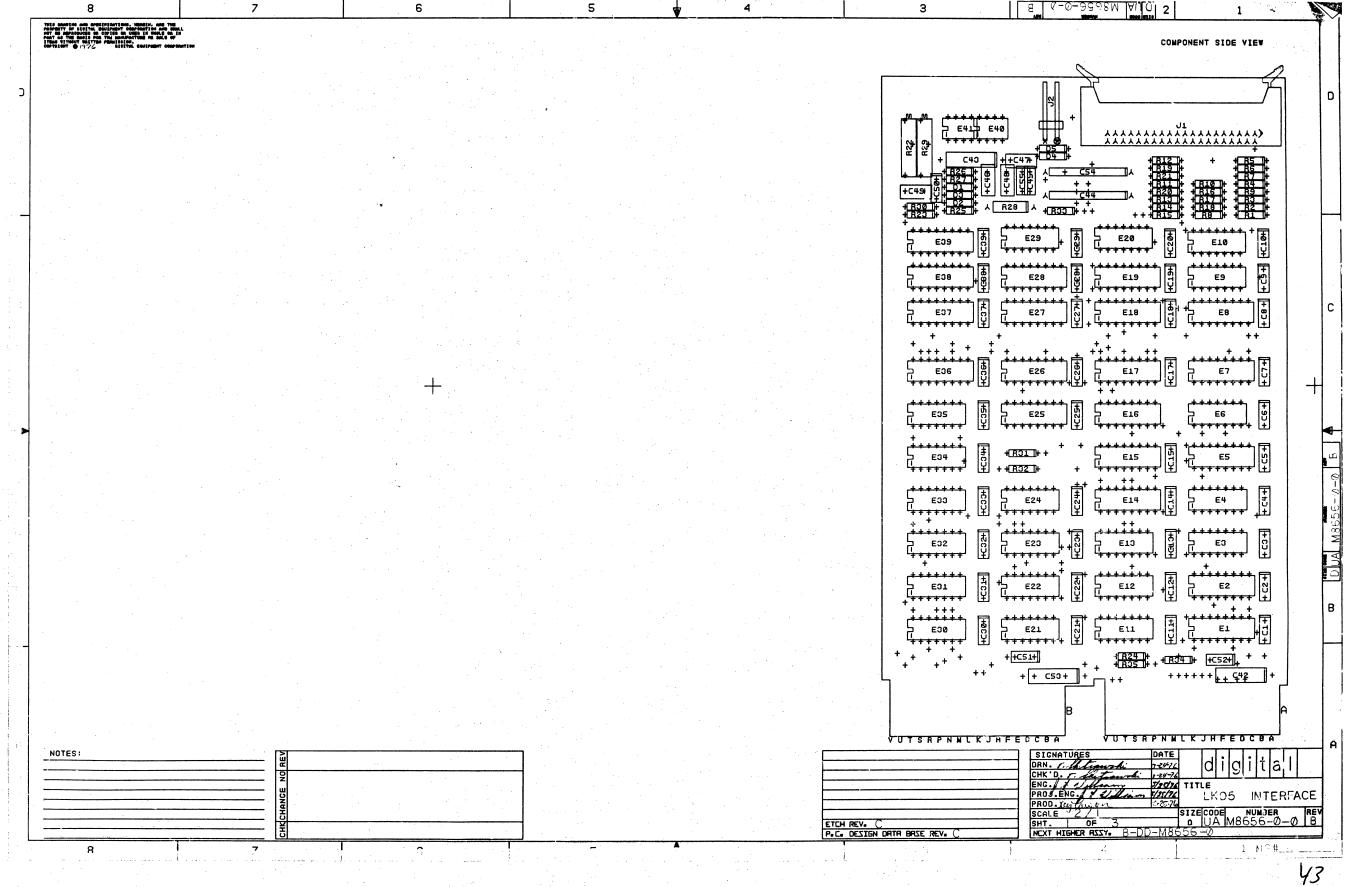
3.5.8 Blank:

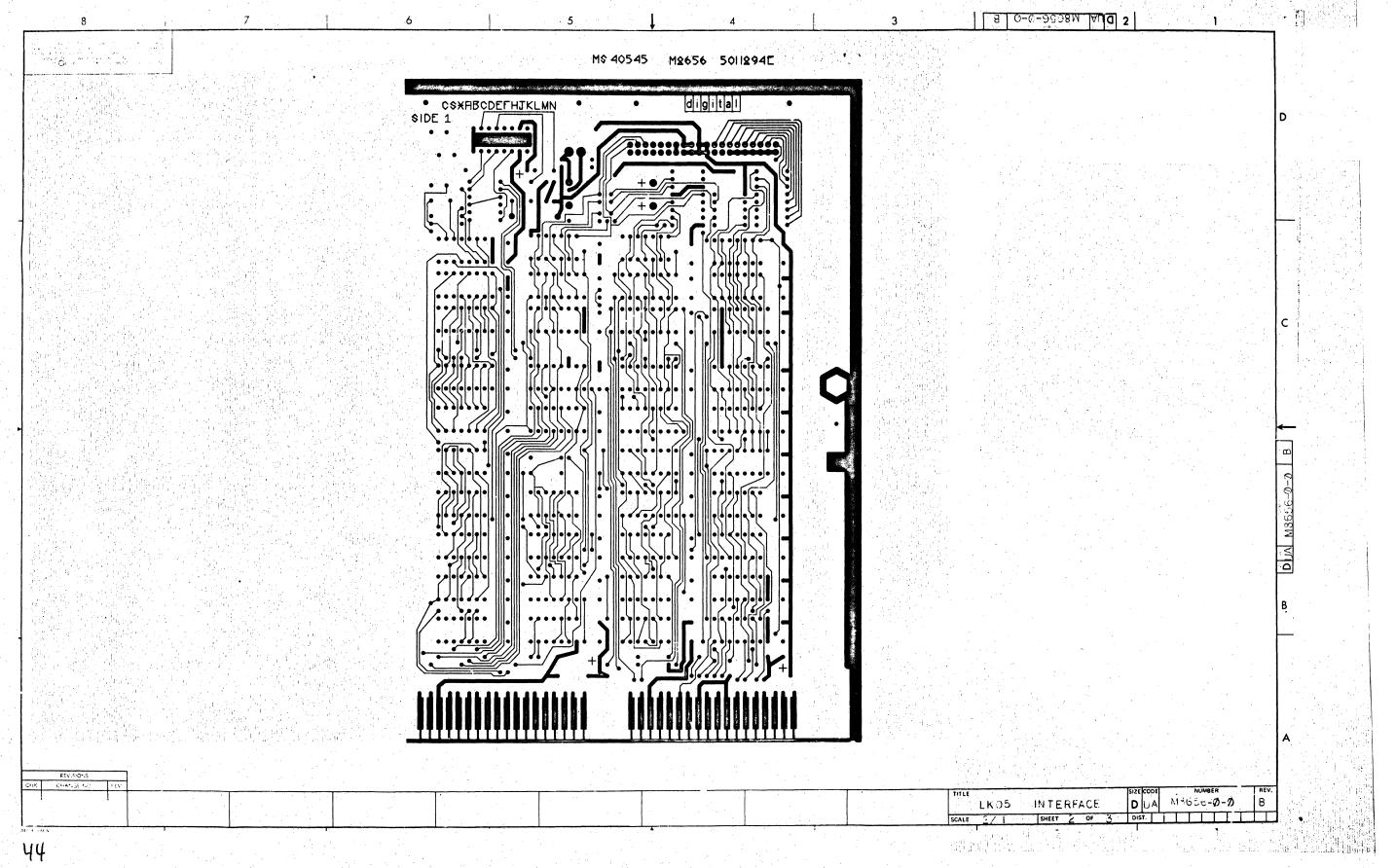
Turns off the display during that display block. This would generally be used to make the display blink.

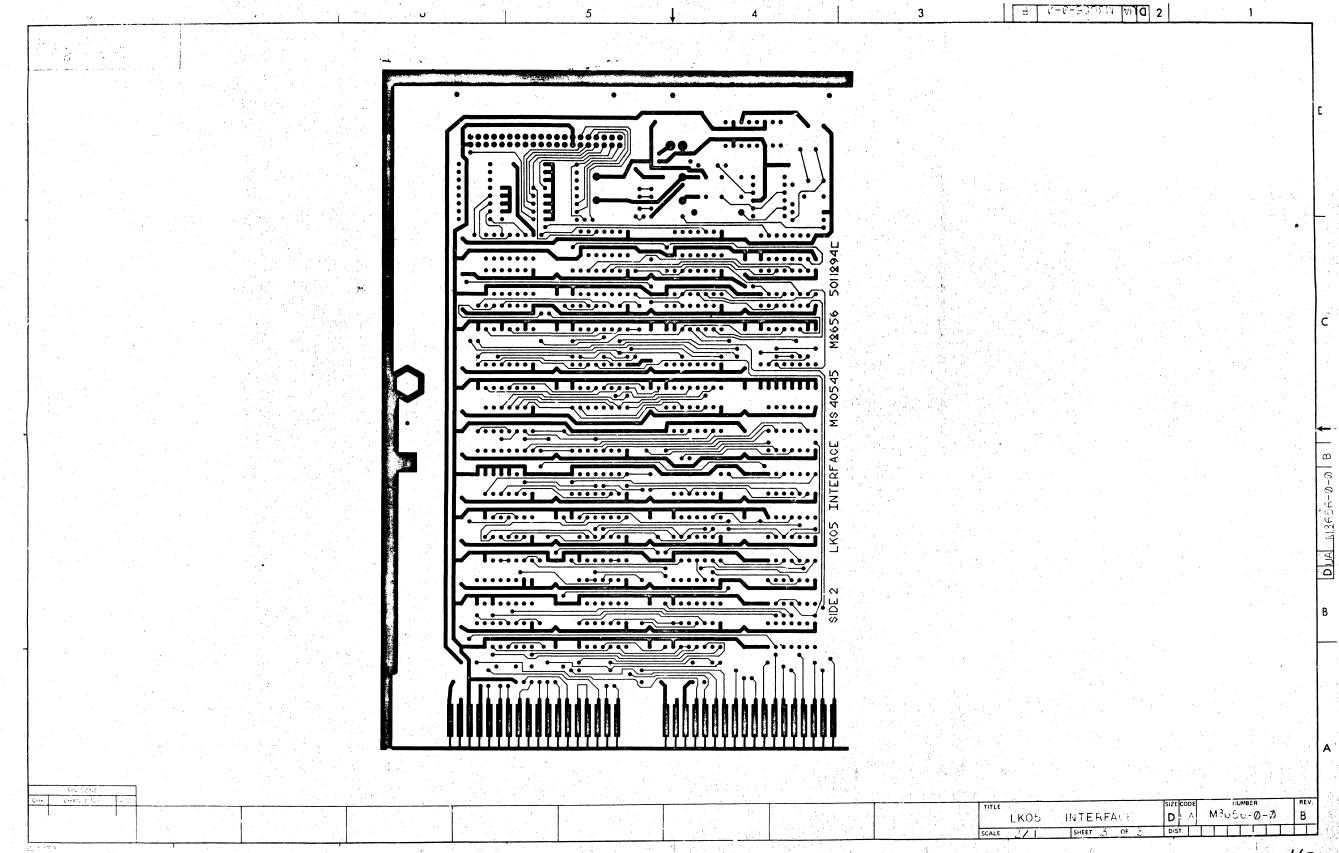
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DEC FORM NO EN-01022-16-N370-(381) DRA 108

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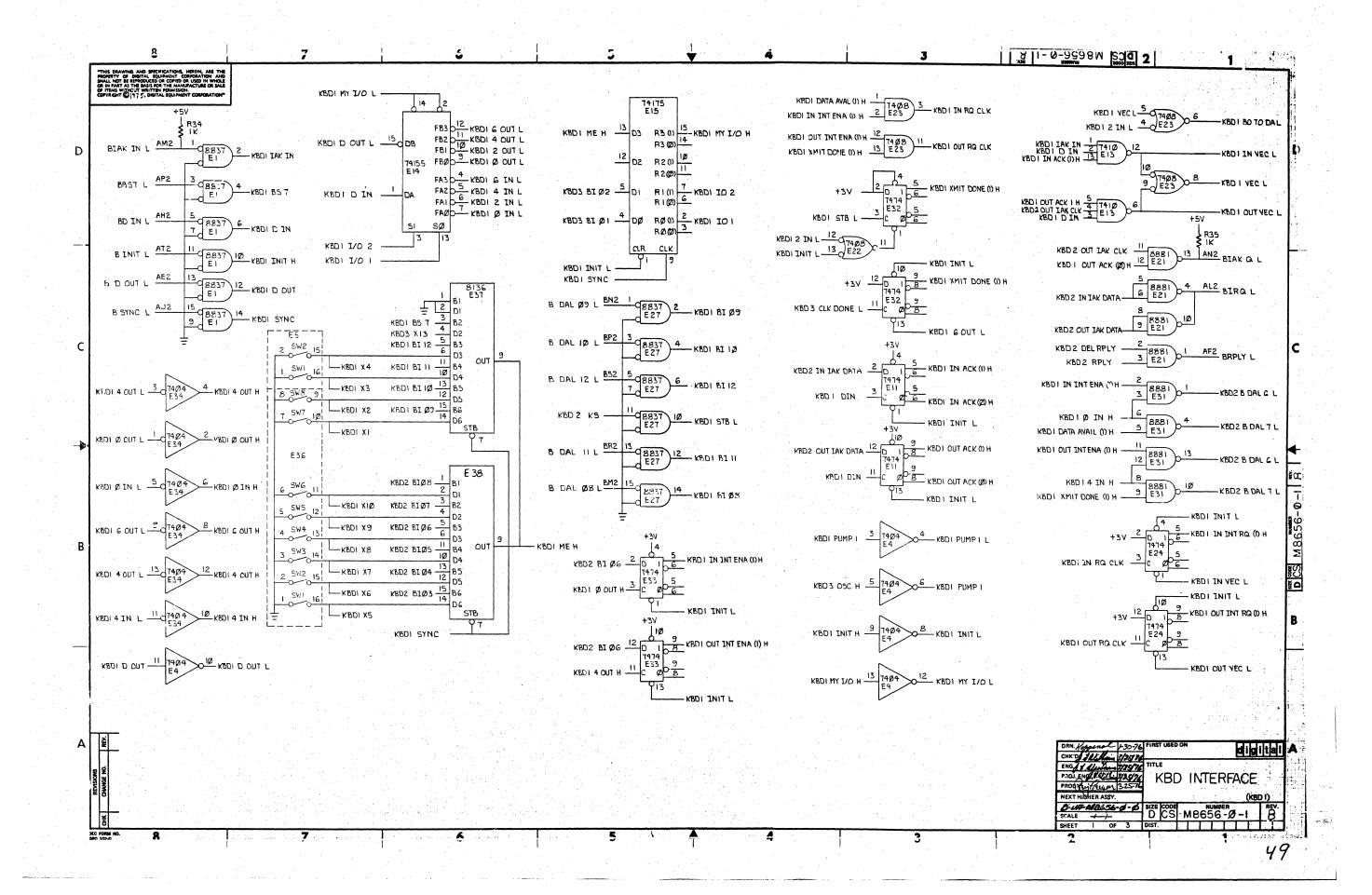


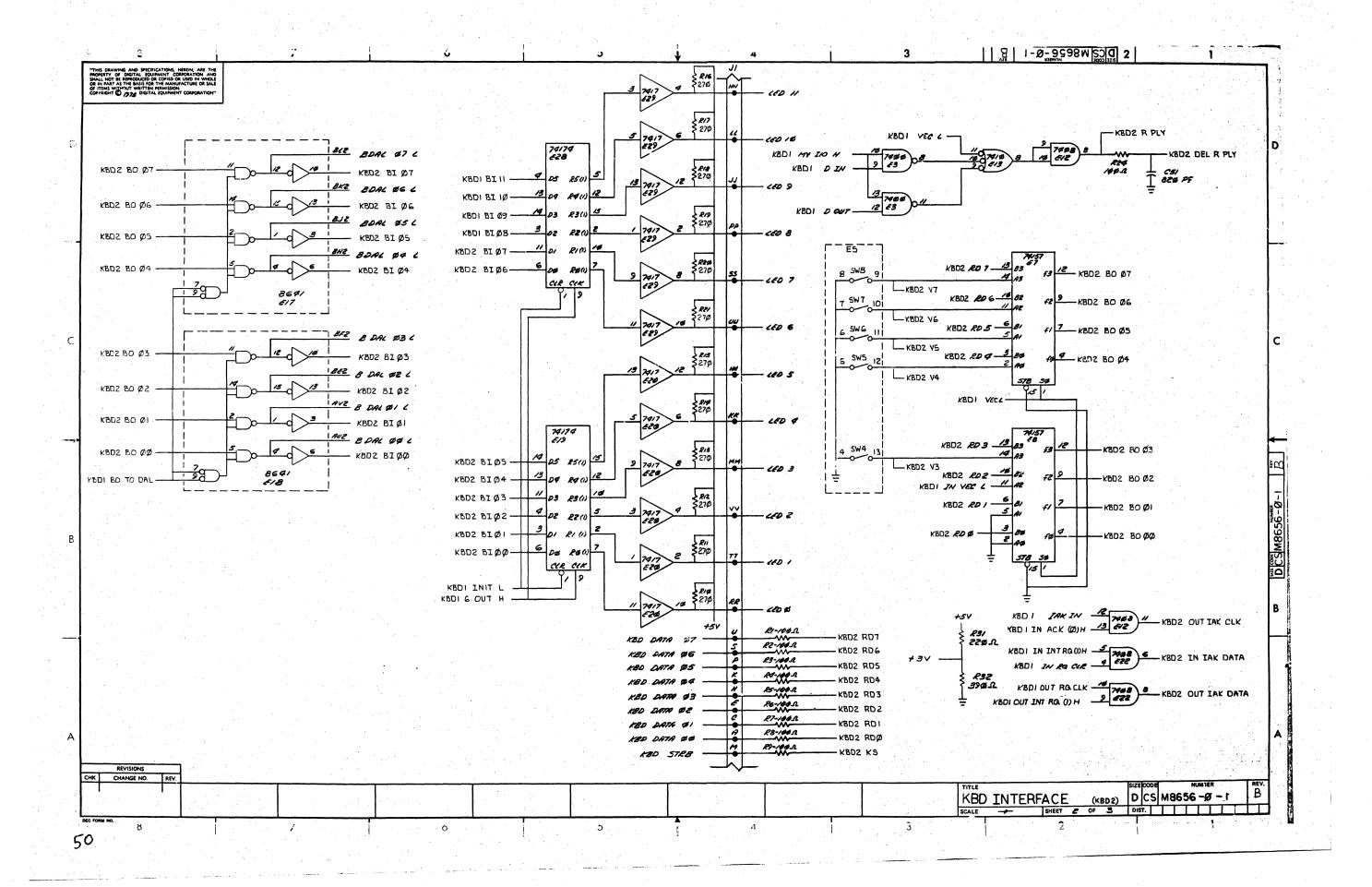


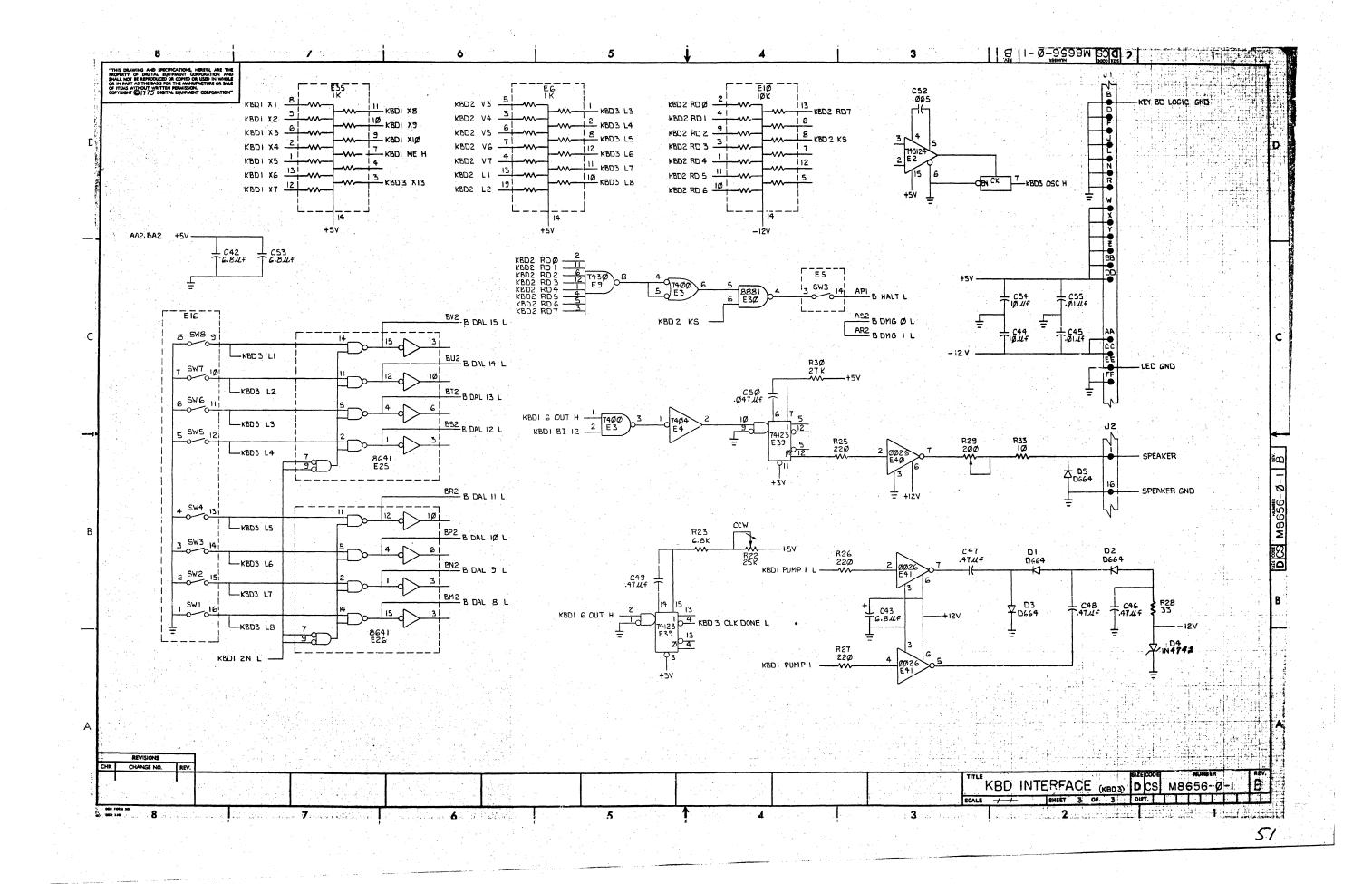
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	DAT		DATE 2-23 PHOD (1) DATE	-76	-								
	ITEM NO.	DRAWING NO.	PART NO.	DESCRIPTION	1	: .					REF DESIGNATION		
	1	D-CS-M8656-0-1		CIRCUIT SCHEMATIC		+ +		$\dagger \uparrow \uparrow$	1-1-	111			
	2	K-CO-M8656-0-4		X-Y COORDINATE LOCATIONS	1-1-	11		17					
	3	D-AH-M8656-0-5		ASSY/DRILL HOLE LAYOUT				-		1111			
	13	B-MII-M8656-0-6		MODULE ECO HISTORY	 	+	_	+					
	5	B-M1-M0030-0-0	5011894	ETCHED CIRCUIT BOARD				++	++-	 			
	6	AND THE RESERVE THE PROPERTY OF THE PROPERTY O	1000027	CAP 820 Pf	11						C51		
	1		1009678	CAP .047 Uf	+-+	+		-			C50		
	8		1003076	CAP 10 Uf	2			++	++		C54, C44		
	9	The state of the s	1001476	CAP .01 Uf	40			╅	+++		C55, C45, C1-C15, C17-C39		
	10	and the state of t	1001010-01	CAP .005 Uf	11		_	+-+			C52		
			1001703	CAP 6.8 Uf	3			╅	+		C43, C42, C53		
	11		1010279	CAP .47 Uf	4			++		+-+-+-	C46, C47, C48, C49		
	12		1100114	DIODE D664	4			++	-+	+-+-	D1, D2, D3, D5		
	13		1100114	DIODE IN4742	$\frac{1}{1}$			+-+			D4		
	14			CONNECTOR	$\frac{1}{1}$			+-+	-++-		J1		
	15		129941-02		3			++			E16, E36, EØ5		
	16		1211164-04	SWITCH	$\frac{1}{1}$		-+	+			R28		
	17		1300195	RESISTOR 33 OHMS 1/2W ± 5%	10						R1-R9, R24		
	18		1300229	RESISTOR 100 OHMS 1/4W ± 5%	4						R25, R26, R27, R31		
	19		1300271	RESISTOR 220 OHMS 1/4W ±5%			_	1-1			R32		
	20		1300309	RESISTOR 390 OHMS 1/4W ±5%	$\frac{1}{1}$			++			R33		
	21		1301317	RESISTOR 10 OHMS 1/4W ± 5%	$\frac{1}{1}$	1		11			100		
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	DRAWING NO.	PART NO.	DESCRIPTION			.					REF DESIGNATION	
22		1301972	RESISTOR 270 OHMS 1/4W ± 5%	12							R10-R21	
23		1301423	RESISTOR 6.8K 1/4W <u>+</u> 5%	1							R23	
24		1309143-12	RESISTOR 25K POT	1							R22	
25		1.300365	RESISTOR 1K 1/4W ± 5%	2	11			1 1	1-1-	1	R34, R35	
26		1305346	RESISTOR 27K 1/4W ± 5%	1	11			11			R30	
27		1905547	IC 7474	4							Ell, E33, E24, E32	
. 28		1905575	IC 7400	1							E3.	
29		1905576	IC 7410	1							E13	
30		1905578	IC 7430	1							E9	
31		1909686	IC 7404	2							E34, EØ4	
32		1909705	IC 8881	3			1			1	E21, E30, E31	
33	* * * * * * * * * * * * * * * * * * *	1909929	IC 7417	2			1	111	111	1	E20, E29	
34		1910155	IC 7408	3						T	E12, E22, E23	
35		1910436	IC 74123	1							E39	
36		1910655	IC 74157	2							E7, E8	
37	-	1910656	IC 74155	1							E14	
38		1911116	IC 8837	2							E1, E27	
39		1911579	IC 8641	4							E17, E18, E25, E26	
40	,	1911911	IC 74S124	1							E2	
41		1912395	IC 8136	2							E37, E38	
42		1912098	IC MH0026C	2		1	1	† †	11	1	E41, E40	
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	MADE BY J. WILLIAMS DATE 9-15-75 ENG J.	PARTS CHECKED T. S DATE 2-23 PROD DATE 3-	HETRAWSKI SECTION										
	TEM DRAWING NO.	PART NO.	DESCRIPTION	1		1		-11				REF DESIGNATION	
	43	9008337-06	HANDLE FLIP CHIP, MAGENTA	1				11					
	44	1212204-00	2 PIN CONN (MALE)	1								Ј2	
	45	1309143-05	RESISTOR 200 POT	1				11				R29	1
	46	1300005-01	RESISTOR PACK 1K OHM	2								E06, E35	
	47	1300005-03	RESISTOR PACK 10K OHMS	1				11		1-1		Elø	1
	48	1910651	IC 74175	1				11	1	11		E15	
	49	1910652	IC 74174	2				+++		11		E19, E28	
	50	9006732	HANDLE EYELETS	2			- 	17		111			
	51	1209941-03	LATCH LEFT	1				111	_				
	52	1209941-04	LATCH RIGHT	1									
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SHEET _1 OF _5

ENG	SINEERING	G SPE	CIFIC	ATION		digirita i		CONTINUATION SHEET	
TITLE	M8656 LKC)5 to 1	LSI-11	Bus Inte	erface				
					_				
3.2	Keyboard St	atus	Registe	r KBSI	<u>R</u>				
	Bit 15-8		Not Us	ed					
	Bit 7		by key been t	/board st	trobe ted fr	indica om the	ting	ly - set to l a character has poard. Cleared by	
	Bit 6		by IN		it 6 i			Write - cleared oit 7 is set, an	
	Bit 5-0		Not Us	sed					
3.3	Keyboard I	oata B	ıffer	KBUF					
	Bit 15-8		Switch	Setable	e ID n	umber			
	Bit 7-0	-	Keyboa	ard Data	bits.				
3.4	Led Status	Regi	ster I	CSR					
	Bit 15-8		Not Us	sed					
	Bit 7							y INIT. Cleared whastable time delay	
	Bit 6			ru			6 is	set and bit 7 ge	ts
	Bit 5-0	•	Not U	sed					
3.5	Led Data B	ıffer	LBUF	4		•			
	Bit 15-13		Not U	sed			:		
: 1	Bit 12		Causes	s an aud	ible c	lick v	hen :	set to a 1.	
	Bit 11-0		Cause	s indivi	dual l	eds to	o ligh	ıt.	
3.6								and one for Leds has priority.	•
• ;									
	-					SIZE	CODE	NUMBER M8656-Ø-8	RE

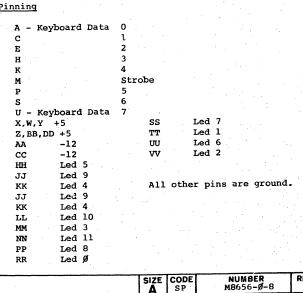
ENGINEERING SPECIFICATION disgritiali CONTINUATION SHEET TITLE M8656 LK05 to LSI-ll Bus Interface 1.1 The M8656 is an interface between the LK05 keyboard and the LSI-11 Bus. 1.2 The M8656 receives, from the LKO5, 8 bit parallel data indicating which key has been struck,. 8 additional bits are jumper selectable and serve as a hardware ID code. It transmits to the LKO5, 12 bits of parallel data, lighting associated Led indicators. A 13th bit is used to cause an audible click. 1.3 Power Requirements +5V at 1.6 A Max./1.1A Typ. +12V at 0.3 A Max./0.2A Typ. 2.1 The module has switch selectable vector and address. The volume of the click pulse, fed to an external speaker, is adjusted via a variable resistor. The time between clicks is also adjustable via a variable A jumper enables the insertion of Halt on the LSI-11 bus. This level is asserted when an 8 bit delete 377/8 is transmitted by the keyboard. An 8 bit switch selectable ID code is available as the high byte of the Keyboard Data Buffer, the low byte being the keyboard data. 3.0 PROGRAMMING 3.1 All software control of the M8656 is via 4 device addresses. The addresses are consecutive and start at 0. Bits 3-12 are switch selectable.

DEC FORM NO DEC 16-(381)-1022-N370 SHEET _2

ENGINEERING SPECIFICATION dingrittall CONTINUATION SHEET M8656 LK05 to LSI-ll Bus Interface 3.7 Address and Vector Assignments The address and vector assignments may be set to the standard console, ie: Vector Address 177560 60/64 62 66 in which case it will interface with the ODT in the LSI-11. However, addresses starting at 76XXXØ and all vectors up to 374 are possible. 3.8 Halt Character

When enabled by a jumper, if 377/8 is transmitted from the keyboard the Halt line on the LSI-11 bus is asserted for 1 MS. This forces the processor into ODT.

4.0 40 Pin Pinning



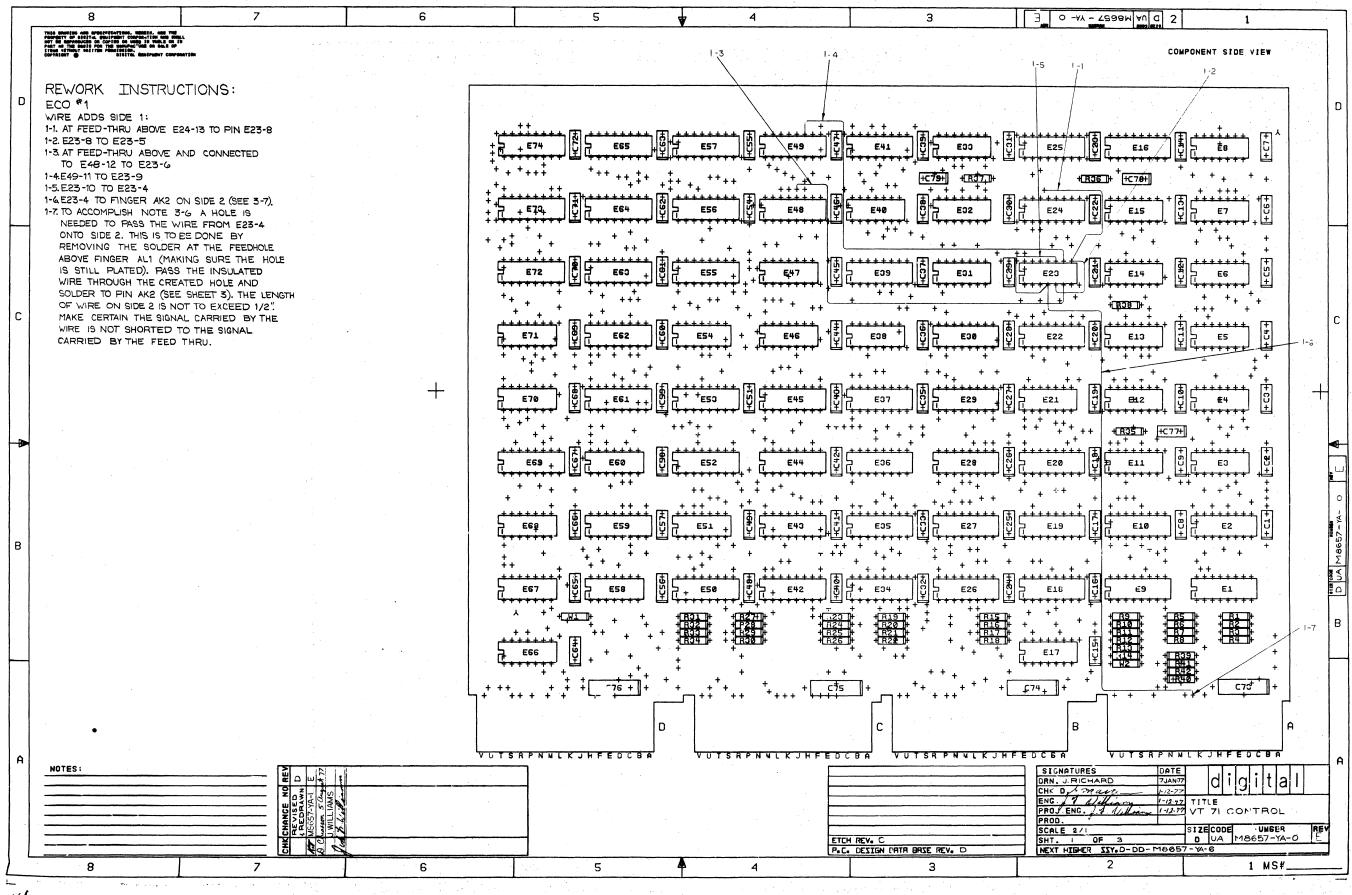
DEC FORM NO DEC 16-(381)-1022-N370 DRA 108 SHEET 4 OF 5

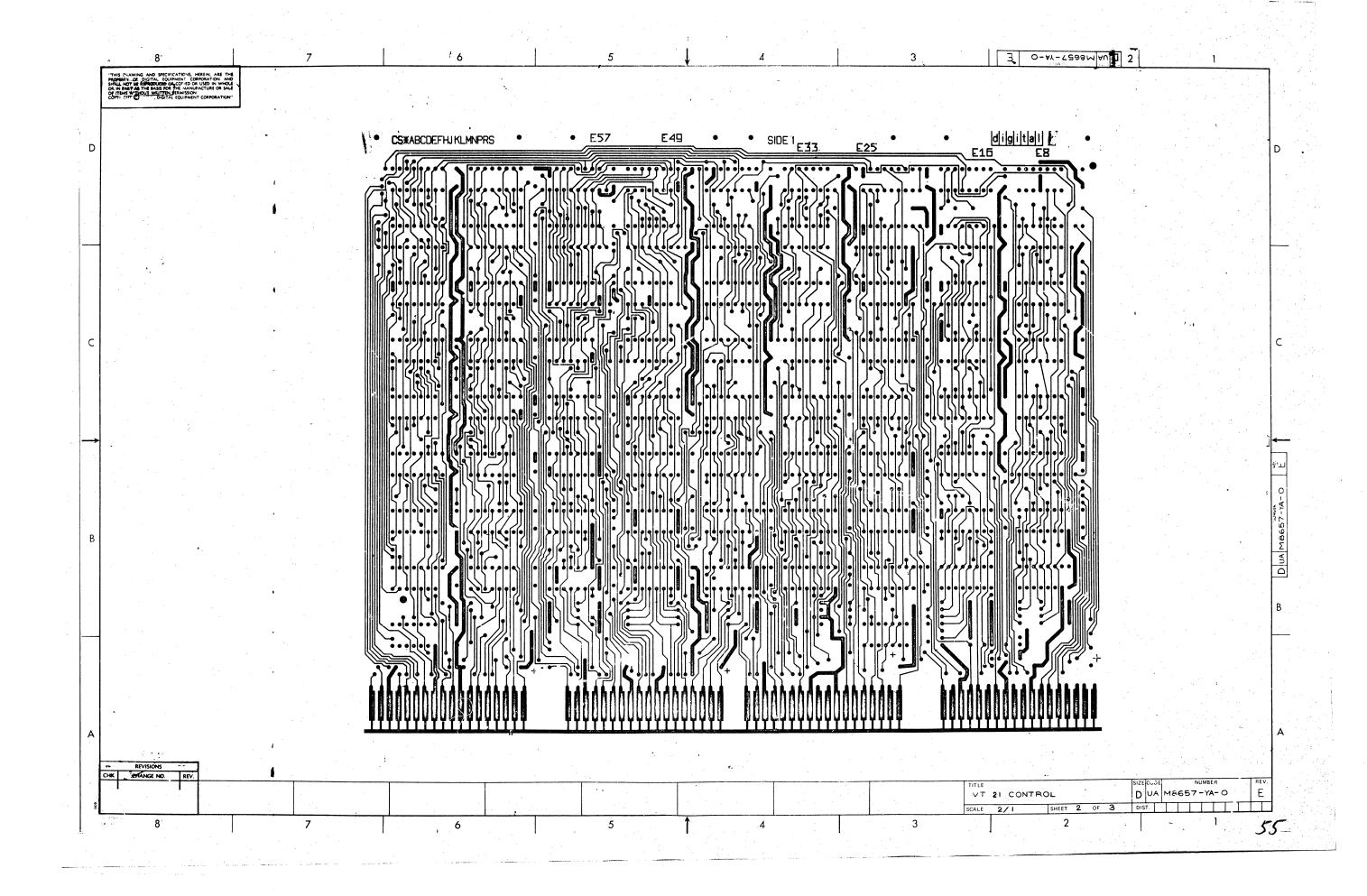
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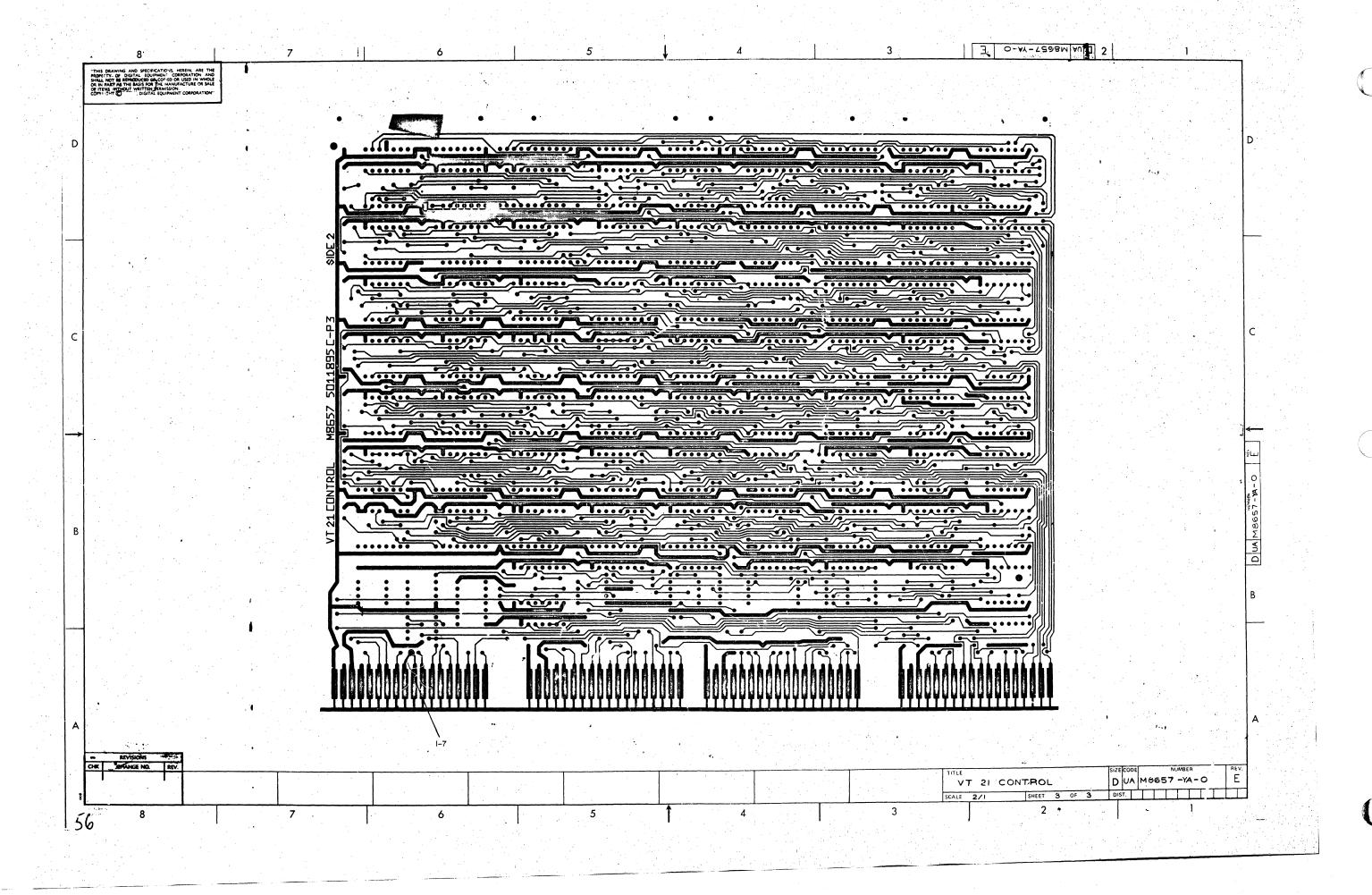
ENG	NEERING	SPECIFI	CATION	digita	0 c	ONTINUATION SHEET	Γ
TITLE	M8 6 56	LK 0 5 to L	SI-11 Bus Int	erface			
5.0	Finger Pin	nina					
3.0	1111901 1111						
	+5	AA2	BIRQ L		AL2		
		BA 2				•	
			· · · · · · · · · · · · · · · · · · ·				
	+12	AD2					
		BD2	BRPLY L		AF2		
	BBS7	AP2					
	BDAL Ø L	AU2					
	BDAL 1 L	AV2	BSYNC L		AJ2		
	BDAL 2 L	BE2					٠.
	BDAL 3 L	BF2	GND		AC2		
	BDAL 4 L	BH2	GND		ATl		
	BDAL 5 L	BJ2					
	BDAL 6 L	BK2					
	BDAL 7 L	BL2	GND		BC2		
	BDAL 8 L	BM2	BDC OK H		BAl		
	BDAL 9 L	BN2					
	BDAL 10 L	BP2		# + N	BTl		
	BDAL 11 L	BR2	UNUSED		AKl		
	BDAL 12 L	BS2			ALl		
	BDAL 13 L	BT2	UNUSED		BK1		
	BDAL 14 L	BU2			BLl		
	BDAL 15 L	BV2	UNUSED		BCl		
•	BDIN L	AH2	UNUSED		BD 1		
	BDOUT L	AE2	UNUSED		BEl	•	
	BHALT L	APl	UNUSED		BFl		
	BIAK I L*	AM2	UNUSED		BHl		
	BIAK O L*	AN2					
	BINIT L	AT2					
	BDMGIL	AR2					
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SHEET 5 OF 5 53



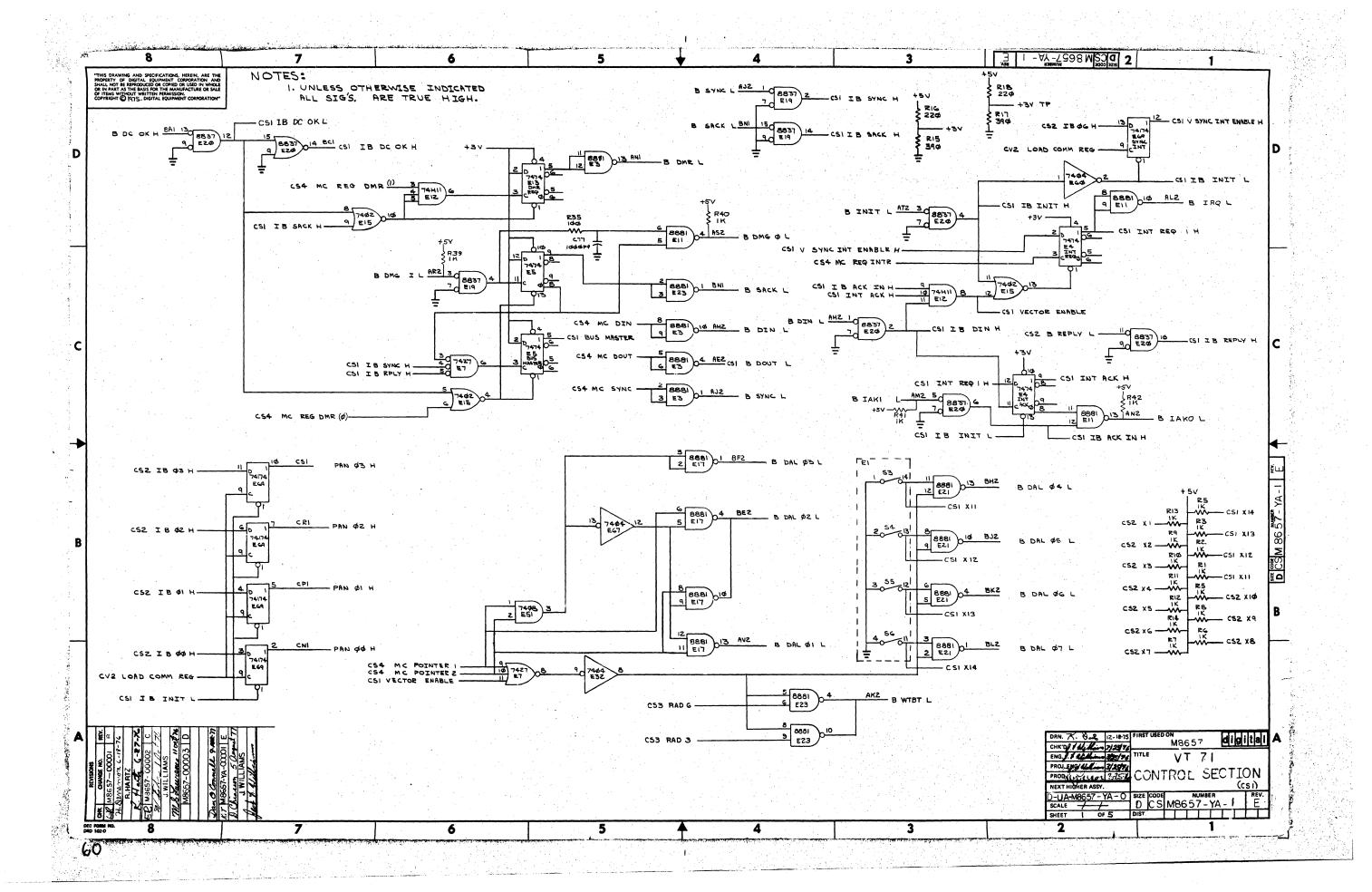


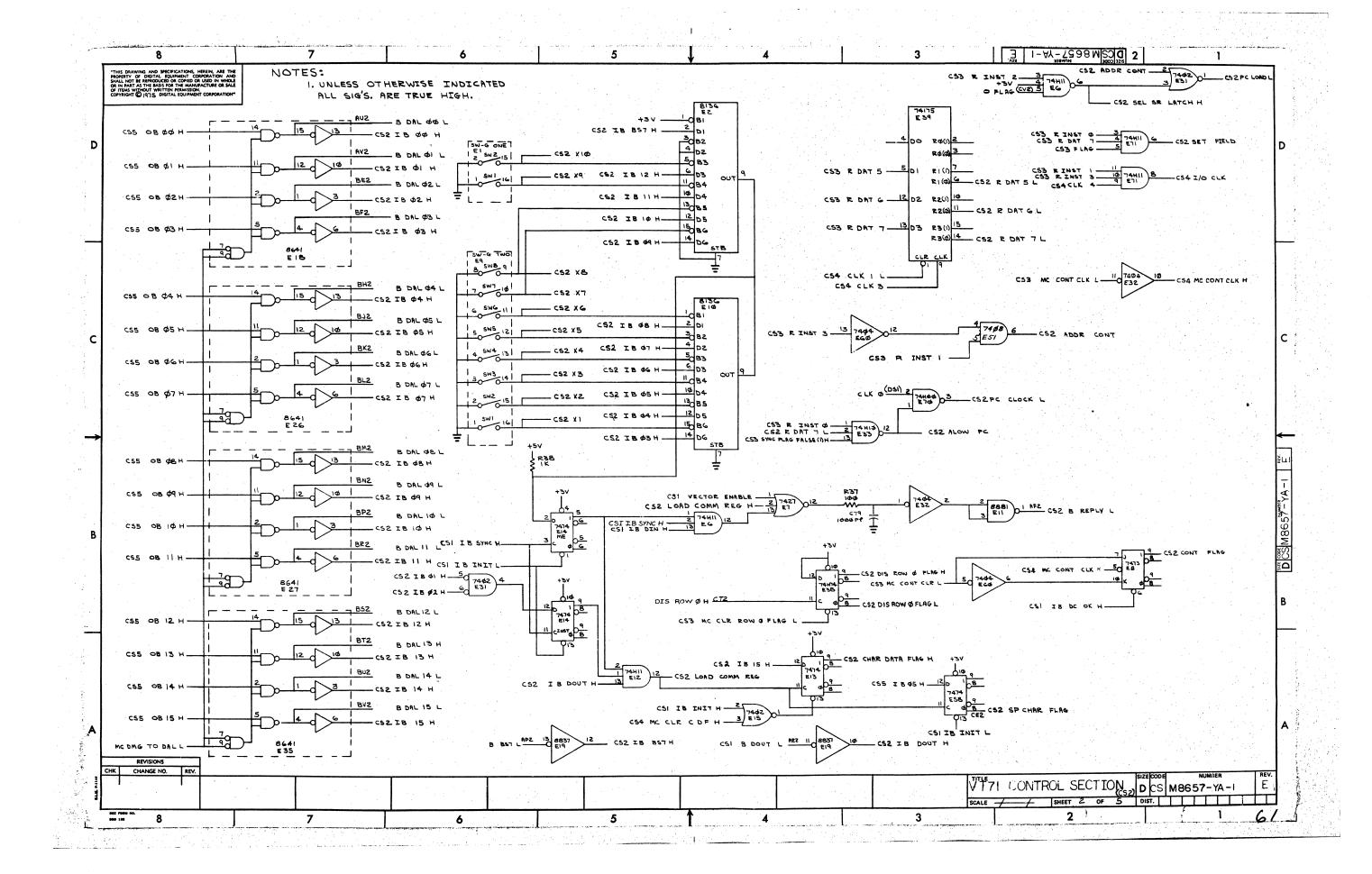


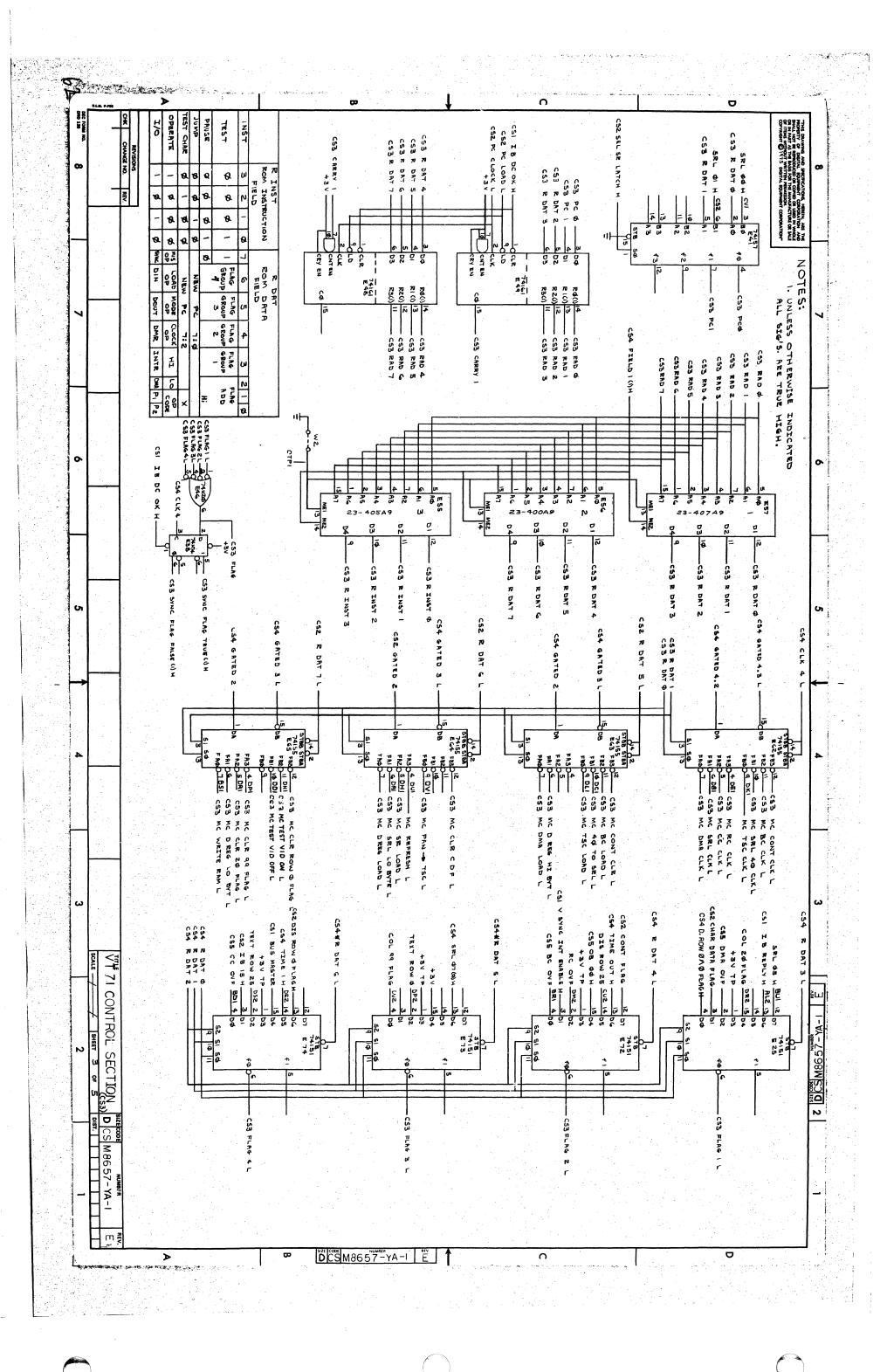
	DIGITAL	EQUIPMENT PARTS	CORPORATION			QU.	ANTIT	Y/VAR	IATION			NOTES:
DATE	BY K. GLEEZEN 2/19/76 3/25/76	DATE PROD CALLED DATE	SECTION 1	657-YA-2								
NO.	DRAWING NO.	PART NO.	DESCRIPTION	M86								REF. DESIGNATION
1		5011895	ETCHED CIRCUIT BD.	1								
2		1000042	CAP1000PF	3								C77, C78, C79.
3		1001610-00	CAP .01UF 50V	68								C1-C33, C35-C49, C51, C54-C72
4		1005306	CAP 6.8 UF 35V	4								C73-C76
5		1300229	RES. 100 1/4W 5%	2								R35, R37
6		1300271	RES. 220 1/4W 5%	2								R16, R18
7 .		1300309	RES. 390 1/4W 5%	2								R15, R17
8		1300365	RES. 1K 1/4W 5%	35								R1-R14, R38, R19-R34, R39-R42
9		13023 9 4	RES.30/K 1/4W 5%	1						·		R36
10												
11		1905547	IC DEC 7474	5								E4, E5, E13, E14, E58
12		1905587	IC DEC 7473	2								E8, E47
13		1909004	IC DEC 7402	2				3.				E15, E31
14		1909056	IC DEC 74HØØ	1								E7Ø
15		1909057	IC DEC 74H1Ø	- 1								E33
16		1909267	IC DEC 74H11	4								E6, E12, E4Ø, E71
17		1909667	IC DEC 74H74	1								E38
18		1909686	IC DEC 74 0 4	3								E32, E54, E6Ø
19		1909705	IC DEC 8881	5		T -				:		E3, E11, E17, E21, E23
20		1909713	IC DEC 8815	1								E68
21		1909931	IC DEC 74HØ4	1	·			_				E67
H8657-1	M8657-3 M8657-74											
HIS DR OCPO3 RKP AS ERMISS	AWING AND SPECIFICATIONS, HE ATION AND SHALL NOT BE REP THE BACS FOR THE MANUFAC	RODUCED OR COPIED O	'C worms/mark series (market) [T/TP 7] / C/ONTIT	ROL SECT	ON			D-UA-M SHEET	18657-YA	-Ø OF	3	SIZE CODE NUILEER E

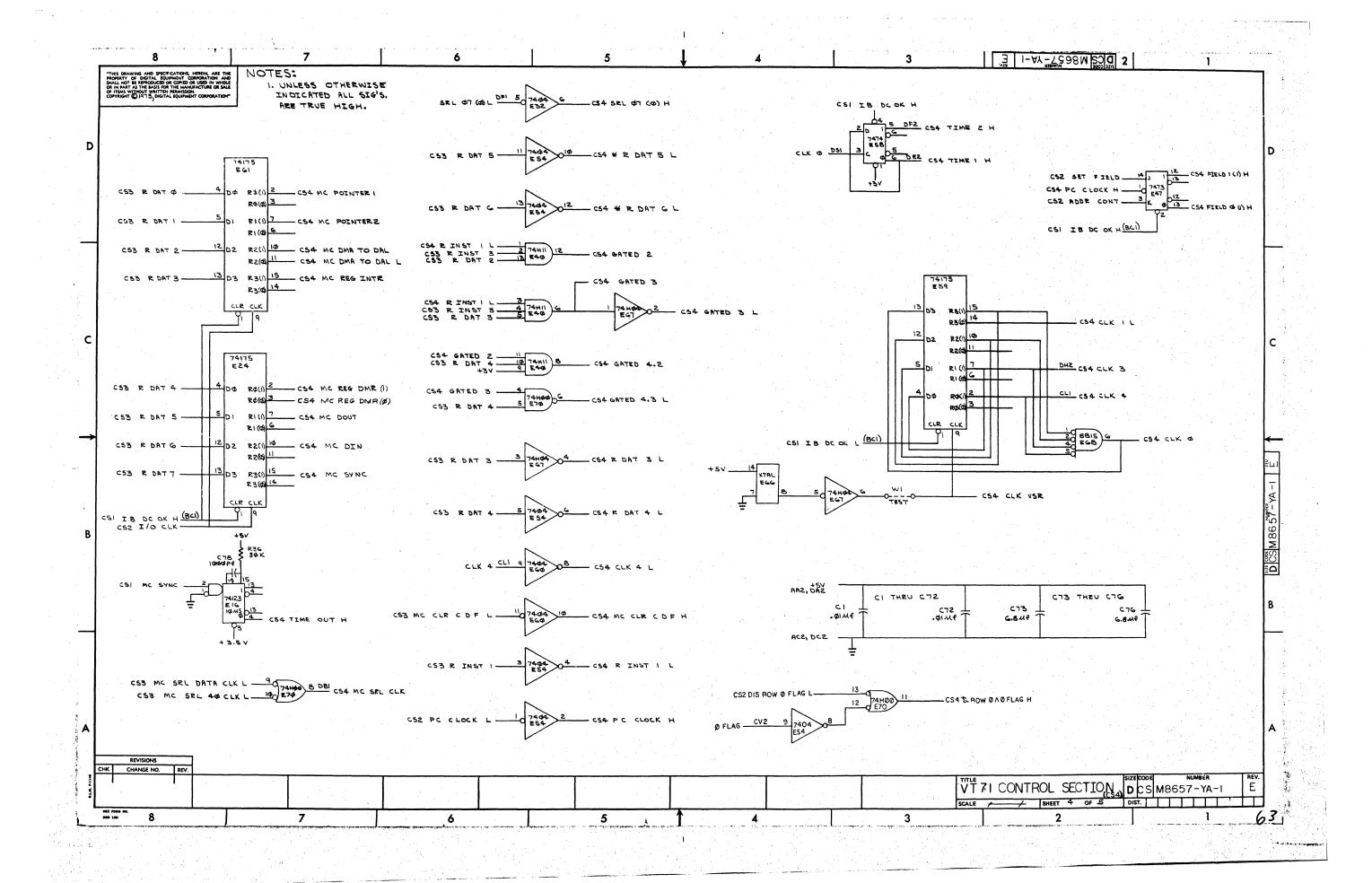
	DIGITAL		TCORPORATION		AUO	NTITY/	VARIA	TION		NOTES:
DATE	BY K. GLEEZEN 2/19/76 3/25/76	PARTS CHECKED K. (DATE PROD CHAPTE DATE	SECTION 1	57-√A-Ø						
TEM NO.	DRAWING NC.	PART NO.	DESCRIPTION	M86						REF. DESIGNATION
22		1909936	IC DEC 74151	4			14.			E25, E72, E73, E74
23		1910155	IC DEC 7408	1						E51
24		1910436	IC DEC 74123	1	,					E16
25		1910650	IC DEC 74161	11						E22, E28-E3Ø, E36, E37, E44, E45, E48, E49, E53
6		1910651	IC DEC 74175	4						E24, E39, E59, E61
27		1910652	IC DEC 74174	1						E69
8		1910655	IC DEC 74157	-1					·	E41
9		1910656	IC DEC 74155	4				7		E62-E65
0		1910878	IC DEC 7427	1						E7
1		1911116	IC DEC 8837	2						E19, E2Ø
2		1911579	IC DEC 8641	4						E18, F26, E27, E35
3		1911330	IC DEC 74173	5						E34, E42, E43, E5Ø, E52
4		1905635	IC DEC 74H2Ø	1						E46
5		1912395	IC DEC 8136	2						E2, E1Ø
6		23407A9	1C DEC 6306	1						E57
7		23400A9	IC DEC 6306	1						E56
8		23405A9	IC DEC 6306	1						E55
9		1811660-03	CRYSTAL OSC KllfØA	1				111		E66
0		9009185	JUMPER INSULATED	2						W1, W2
1		9008337-06	HANDLE FLIP CHIP	4						
HIS DR	AWING AND SPECIFICATIONS. HE ATION AND SHALL NOT BE REP 5 THE BAS'S FOR THE MANUFAC COPYRIGHT F3 107	RODUCED OR COPIED	OR USED IN 1/40LE OR IN VI	T71 CONTROL SEC	II ON		ASSY NO D-UA-ME SHEET	365 7-YA	ø) F 3	SIZE CODE NUMBER GEV. B PL M8657-YA-0

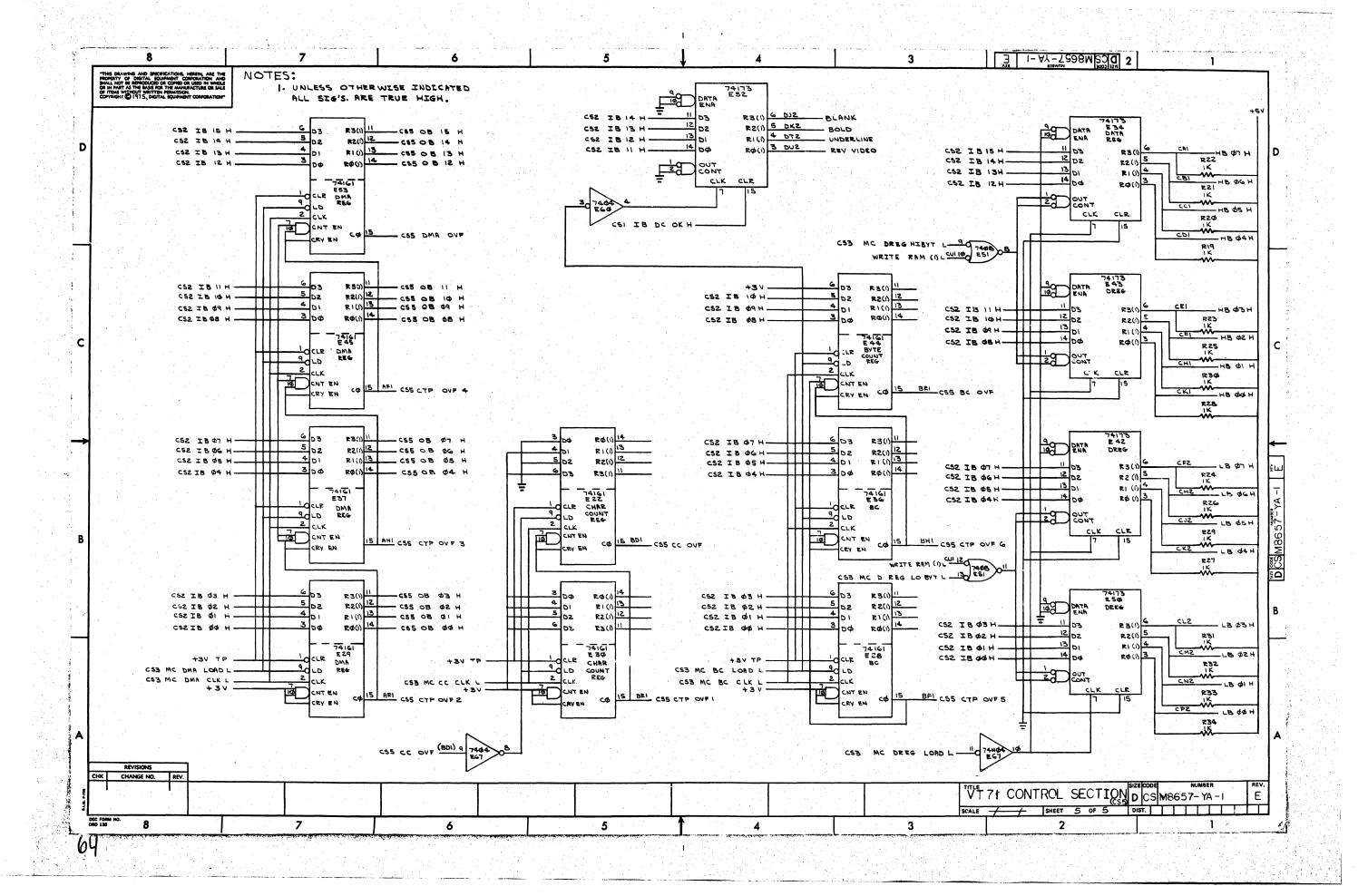
MADE BY N. GLEEZEN DATE 2070 DATE 20	DATI	DIGITAL EQUIPMENT CORPORATION PARTS LIST					401	1111	117/	VAR	CIAI	ION		NOTES:
42 9006732 EYELET GS4-7 8 ELL ELL ELL ELL ELL ELL ELL ELL ELL E	ENG Dati	2/19/76 .	DATE PROD XILL COLOR	SECTION 1 ISSUED SECTION	57-YA-0					٠				
43 121164-04 SWITCH D.I.P. 2	ITEM		PART NO.	DESCRIPTION	M86						1			REF. DESIGNATION
	42		9006732	EYELET GS4-7	8									
	43		1211164-04	SWITCH D.I.P.	2									E1, E9
	E.C.O. NO													









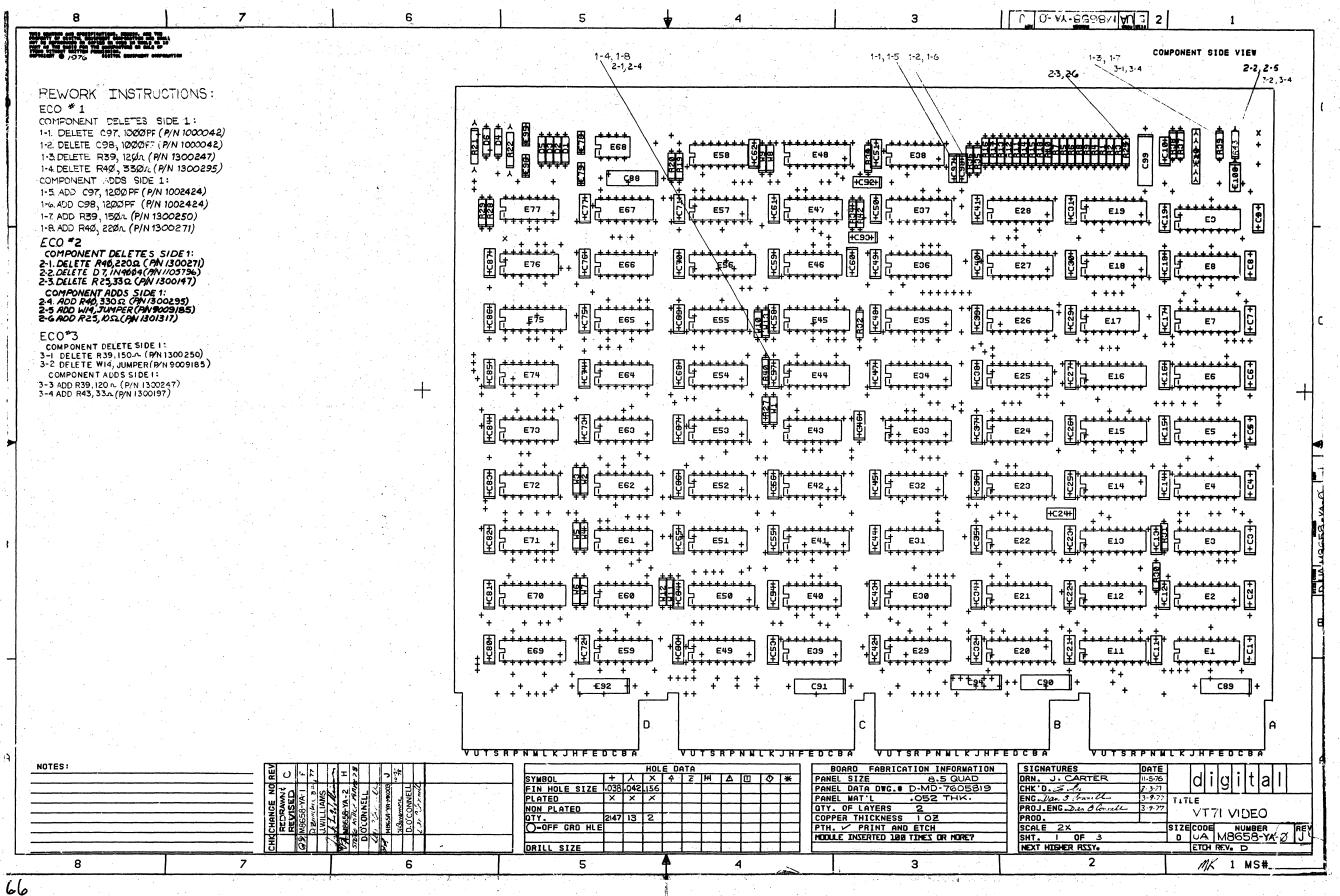


ENGINEERING SPECIFICATION TITLE M8657 CONTROL MODULE REV DESCRIPTION CHG NO ORIG DATE APPD BY DATE APPD BY DATE SIZE CODE NUMBER M657-9-8			MAYNARD, N	MASSACH	IUSET	TS		
REV DESCRIPTION CHG NO ORIG DATE APPD BY DATE	ENG	GINEERING SP	PECIFICATION	٧			DATE 1/12/	76
REV DESCRIPTION CHG NO ORIG DATE APPD BY DATE	TITLE	M8657 CONTROL	MODULE					
			RE					
ENG & William APPD William SIZE CODE NUMBER REV	REV	DESCRI	PTION	CHG NO	ORI	G DATE	APPD BY	DATE
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DEC 16-(392)-1079A-R873 SHEET 1 OF 3	ENG	d & Nollins	gra willing		SIZE (18657-Ø-8	

DIGITAL EQUIPMENT CORPORATION

ENGINEERING SPECIFICATION CONTINUATION SHEET M8657 CONTROL MODULE 1.1 The M8657 is a control processor interface between the VT21 Video Module(M8658) and the L3I-11 Bus. It is both a DMA and INT. device. 1.2 The M8657 receives, from the M8658, all status information required to control the raster scar display. It transmits to the M8658, 16 bits of address and data, control and 1.3 POWER REQUIREMENTS: +5VDC AT 4.1 A MAX./3.0 A TYP. 2.1 The module has switch sclectable vector and device address. There are three other addresses which will be called pointer addresses. They are consecutive and will follow the selected 3.0 DEVICE, VECTOR AND POINTER ADDRESS Switch Off = $1/On = \emptyset$ Device <u>Vector</u> Pointer 1 Pointer 2 Pointer 1 & 2 177670 364 366 370 4.0 FINGER PINNING B DMG I L *
B DMG O L *
B INIT L +5VDC AR2 CC2 -CJ1 AS2 AT2 BA2 DA2 CMl B DAL Ø L AU2 B DAL 9 L
B DAL 1 L
B DAL 2 L
B DAL 3 L
B DAL 4 L +12VDC AD2 DC2 BE2 BD2 CD2 DMl BH2 DD2 B DOUT L B DAL 6 L BK2 AE2 GND AC2 B RPLY L AJ1 B DIN L AH2 B DAL 8 L BM2 B DAL 9 L B DAL 1ØL AMl BN2 B IRQ L
B IAK I L*
B IAK O L* AT1 AL2 BP2 BC2 BJ1 AM2 B DAL 11L BR2 AN2 B DAL 12L BS2 B DAL 13L SIZE CODE SP NUMBER M8657-Ø-8 DEC FORM NO DEC 16-(381)-1022-N370 DRA 108 SHEET 2 OF 3

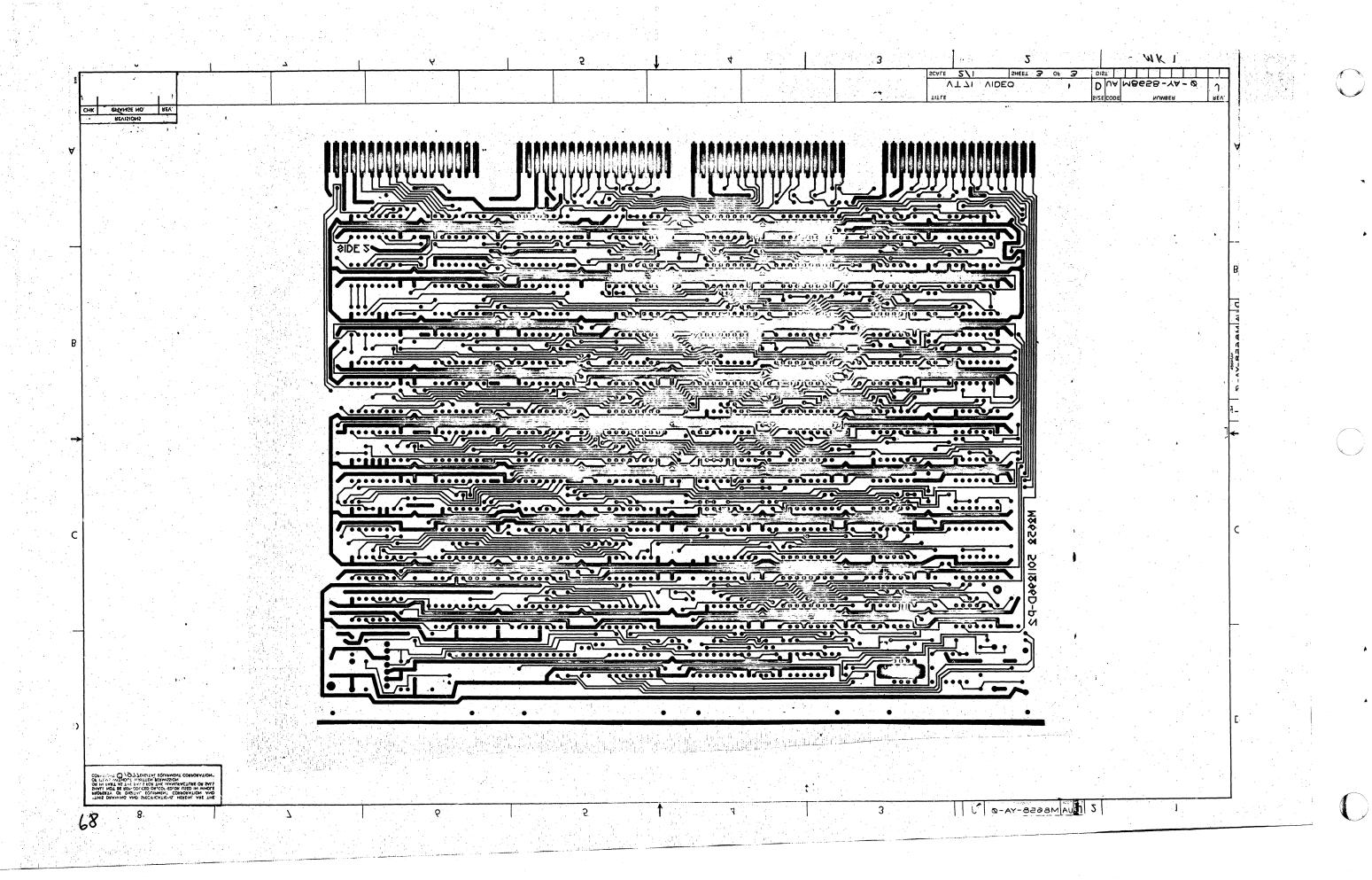
ENGINEERING S	PECI	FICATION	নি তি শিক্ষা ব		CONTINUATION SHI	EET
TITLE M8657 CONTRO	MODU	LE				
B DAL 14L	BU2	TEXT ROW 25	DS	52	нв Ø3 н	CEL
B DAL 15L	BV2	UNDERLINE	מם		нв Ø2 н	CF1
SP CHAR. FLAG	CE2	REV. VIDEO	Dt	J2	нв Ø1 н	CH1
LВØ7 Н	CF2	COL 99 FLAG	DV	72	нв ØØ н	CKI
LBØ6 H	CH2	DMA OVF	AE		CLK 4	CLl
LBØ5 H	СЈ2	CTP OVF 4	AF	71	PAN ØØ	CN1
LBØ4 H	CK2	CTP OVF 3	AF		PAN Ø1	CPl
LB ₀ 3 H	CL2	B DMR L	AN		PAN Ø2	CRI
LBØ2 H	CM2	CTP OVF 2	AF	12	PAN Ø3	CSl
LBØ1 H	CN2	CTP 1	AS		WRITE RAM(1) L	CUL
LBØØ H	CP2	CLK 1 L	AV	71	SRL ØØ H	CV1
DIS. SCAN Ø	CR2	BDCOK H		_	MC SRL LO BYTE	
SRL Ø1H	CS2	IB DCOK H	BC		MC SRL CLK	DB1
DIS.ROW Ø COL20		CC OVF	BE	-	MC 40+SRL L	DCl
DIS. ROW 25 H	CU2	CTP OVF 1	BE		MC T.VID OFF L	
Ø FLAG	CV2	CTP OVF 5	BF		MC CLK RC L	DEL
TIME 1 H	DE2	CTP OVF 6	BE		SRL Ø7 (Ø) L	DF1
TIME 2 H	DF2	B SACK L	BN		MC LOAD SR	DH1
CLK 3	DH2	BC OVE	BR		MC TSC CLK L	DK1
BLANK	DJ2	MC WRITE RAM			MC TSC LOAD L	DLL
BOLD	DK2	SRL Ø5 H		_	MCT. VID ON L	DNI
CLK VSR	DL2	+3V-CTP				
RC OVF	DM2	HB Ø7 H	CA	_	MC CLR 20 FLAG	
SCAN Ø PLAG	DN2	HB Ø6 H	1		CLK Ø	DSI
TEXT ROW Ø	DP2	HB Ø5 H	Icc		MC REFRESH L	DUL
COL 20 FLAG	DR2	нв ø4 н	CE			DUL
COD EO FERG			1	_		
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* These sig	mals a	are not bussed - !	They a	re d	laisy chained.	
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NOTE: 2						
		pins are unused L	5I-ll	bus	lines and must	
not be u	ısed.	1.1				
		•		\$ c		
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				ODE	NUMBER M8657- 6 -8	RE
		1		SP		· E



£52 CSXABCDEFHUKLMNPRS E22 SIZE CODE NUMBER REV.

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DIST. VT71 VIDEO SCALE 2/1 SHEET 2 OF 3 67

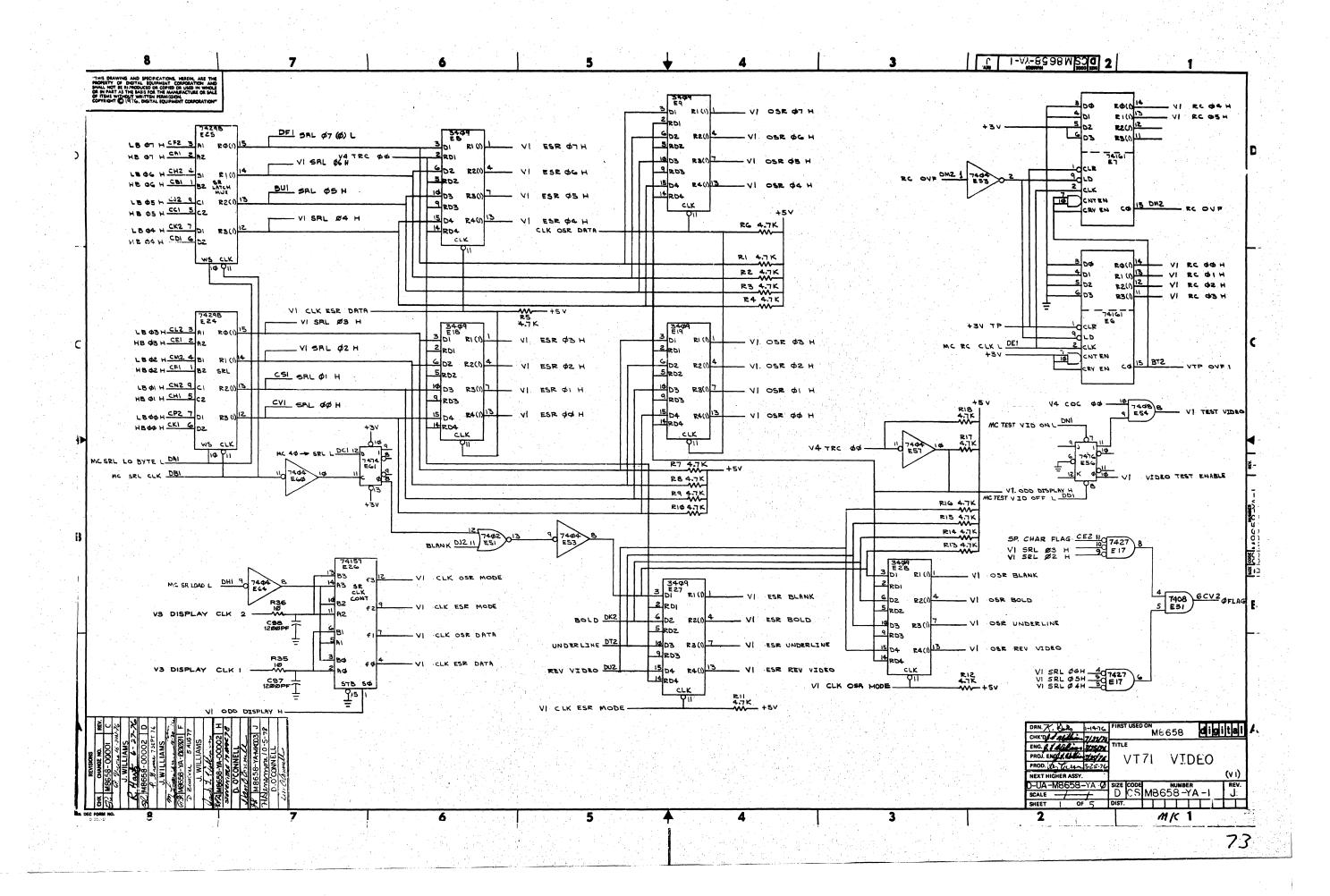


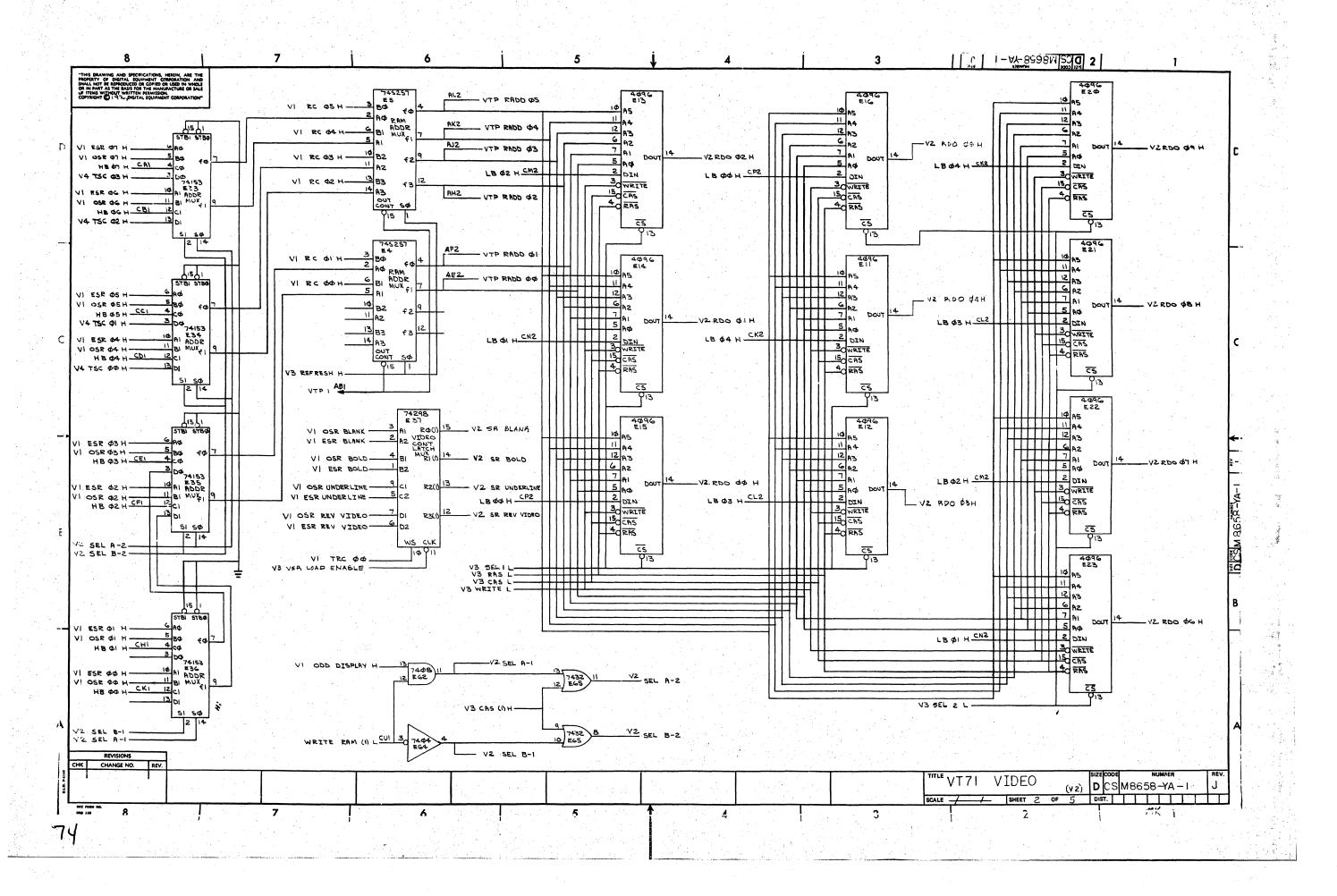
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		PARTS	LIST				TT					
DAT	E BY J. WILLIAMS E 11-10-75	CHECKED J. 1 DATE 2-2	4-76	_								
ENG	J. 8 Nilliam.	PROD WELL 3-2	ISSUED SECTION 1	658								
ITEM NO.	DRAWING NO.	PART NO.	DESCRIPTION	M8(ļ			REF DESIGNATION
1	CS-M0(58-0-1		CIRCUIT SCHEMATIC	1			171					
2	K CO M8658 0 1		X-Y-COORDINATE HOLE LOCATION								1	
3	-D -NH- M8658 - 0-5		ASSY/DRILL HOLE LAYOUT								<u> </u>	
4	B MI M8658 0 6		MODULE ECO HISTORY			1						
5		5011896	ETCHED CIRCUIT BOARD			\dashv	11					
6		1009678	CAP .047 Uf 16V	1	17		11					C93
7		1001610-00	CAP .01 Uf	65								C1-C7, C17, C100, C42-C51, C53-C59, C80-C87, C10, C12, C14, C16, C26, C29, C37-C41
9		1010279	CAP .47 Uf	20								C8, C9, C11, C13, C15, C18, C19, C C79, C95, C96, C32, C27, C21-C25, C31
10		1000042	CAP 1000 Pf	1			11		1			C52
11		1100114	DIODE D664	4	f-f	_	11	_	1 -	1-1	+	D1, D2, D3, D5
12		1109502	DIODE IN4742	1	+-+		++		 	+-+		D6
13		1110994	DIODE IN751A	1	++	-	++		 	+-+		D4
14		1300195	RES. 33 OHMS 1/2W 5%	1	t		++		 	+	_	R21
15		1300197	RES. 33 OHMS 1/4W 5%	2	-		+++		 	+-+		R32, R43
16		12000.2	RES. 12 C OHMS 1/2W	1	f		1		1-1-		_	R22
17	- material discount of the first transfer of the transfer of t	1300243 1300271	RES. 220 OHMS 1/4W 5%	4	+		1-1	_	 	+-+		219, R20, R28, R30 _,
18	, ,	1002424	CAP 1200 pf	2	1 1		111			1		C97, C98
19		1300309	RES. 390 OHMS	2								R29, R31,
20		1300447	RES. 4.7K	20	1							R1-R18, R27,R42
THIS	THE PROPERTY OF THE PROPERTY O	EREIN. ARE THE PROPE PRODUCED OR COPIED O	RTY OF DIGITAL EQUIPMENT TITLE REUSED IN WHOLE OR IN VP77 1	/IDEO	1			ASS	Y NO. D-UA- J	M8658	-YA-Ø	SIZE CODE NUMBER B PL M8658-YA-Ø

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DAT	E BY J. WILLIAMS E 11-10-75	PARTS CHECKED J. DATE 2- PROD GOT YA DATE	24-76	SECTION ISSUED SECTION				. :						
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NO.	DRAWING NO.				+			+	-		+-		, a	
21		=1300417 =1503100		OR 3009R										
23		1905547	I.C., 74		6									E59, E61, E73, E74, E76, E77
24		1905576	IC. 7410		1									E58,
25		1905577	IC. 7420		3	1	ĺ.							E40, E71, E72
26		1905578	IC. 7430		1								.	E63
27		1905585	IC. 7476		2									E56, E75
28		1909004	IC. 7402		2									Ē51,38
29		1909056	IC. 74H0	00	1									E47
30		1909267	IC. 74Hl	1	2									E52, E66
31		1909686	IC. 7404		5									E42, E53, E64, E57,∈60
32		1909937	IC. 7415	3	4									E33-E36
33		1910011	IC. 7486	and the second second	1									E55
34		1910155	IC. 7408		4									E31, E39, E54, E62
35		1910623	IC. 7419		3	1. 1								E1, E2, E3
36		1910650	IC. 7416	1	10									E6, E7, E29, E30, E41, E44, E45, E50 E69, E70
37		1910655	IC. 7415	7	2									E26, E49
38		19-10878	IC. 7427		2					-				E17, E46
39		1911271	IC. 7429	8	3			1						E24, E25, E37
40		1911521	IC. 7432		1		\				1			E65
91 92		1913068								- 1-				
ECO.								•					· .	T
CORP	DRAWING AND SPECIFICATIONS. HE ORATION AND SHALL NOT BE REPI AS THE BASIS FOR THE MANUFAC ISSION COPYRIGHT (2) 1970	REIN, ARE THE PROPE RODUCED OR COPIED (TURE OR SALE OF ITE	ERTY OF DIGITAL EC OR USED IN WHOLE MS WITHOUT WRITE	E OR IN VI	71 VI	DEO .			Ľ	ASSY N D-U	I O. A-M86	58 - YA	-0	SIZE CODE NUMBER R BPL M8658-YA-O
PERM EN-01	ISSION COPYRIGHT © 1970	6 DIGITAL EQUIPM	ENT CORPORATION							HEET	2	OF	4	INSERTION PARTS LIST DATA BASE REV
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ORAWING NO. PART NO. DESCRIPTION	ATE NG	11-10-75 Q. 2 William	PHOD Roy P	4-76 1 ISSUED SECTION	-1 1 1					
ORAWING NO. PART NO. DESCRIPTION	the control of the co	3/25/76	DATE 3	-25-76 1	₩ 88					4
13	40.	DRAWING NO.	PART NO.	DESCRIPTION	Σ W				REF DESIGNATION	_
14 2112154 IC. 3409 6 8 8. E9, E18, E19, E27, E28 191641 IC. 745257 2 8 E4, E5 1910436 IC. 74123 1 1 8 E48 17 1212104-00 CONN. RT ANG. 7 FIN 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	12 l		2112726	IC. 4096 RAM	10				E11-E16, E20-E23	
1911641 IC. 748257 2 B4, E5 16 1910436 IC. 74123 1 E48 17 1212104-00 CONN. RT ANG. 7 PIN 1 E10 18 1302391 RES. 20K 1/4W 5% 2 R33, R34 19 1806229 RES. 1100 ONURS. 1/4W, 5% 1 P32 50 1005306 CAP 6.8 Uf 6 C88C92, C94 51 100002! CAP 220 Pf 1 C60 52 906837-06 HANDLE, MAGENTA 4 53 9006732 HANDLE, MAGENTA 4 54 9009185 JUMPERS, INSURED 13 55 190667 IC. 74474 1 E67 56 1909913 IC. 74H04 1 E32 57 1-1000064 CAP, 105417 207 15V 1 C1054 58 1003340 D1006 EAR 5.0 S. W. S.	13 1		1.		1					
1910436			1 1							
17					2		1 1 1			
18										
1909229 RES. 160 OHMS. 1/4W, 5% 1				and the second of the second o	2					
1005306 CAP 6.8 Uf 6 CAP 6.8 Uf 6 CAP 6.8 Uf 1000021 CAP 220 Pf 1 C60 1000021 CAP 220 Pf 1 C60 22 9008337-06 HANDLE, MAGENTA 4 WILLIAM STATE S										
100002 CAP 220 Pf 1										
52 9008337-06 HANDLE, MAGENTA 4 53 9006732 HANDLE, MAGENTA, EYELETS 8 54 9009185 JUMPERS, INSULATED 13 55 1909667 IC. 74H74 1 56 1909931 IC. 74H04 1 57 1000084 CAR, 150Uf 207 15V 1 58 103340 DIODE, 7ENER 8.8V 57, IW 1 59 1000085 RES IX 1/4 W 5% 2 59 100085 RES IX 1/4 W 5% 2 59 100085 RES IX 1/4 W 5% 3 50				the control of the co						
9006732 HANDLE, MAGENTA, EYELETS 8 9009185 JUMPERS, INSULATED 13 1909667 IC. 74H74 1 1 E67 56 1909931 IC. 74H04 1 57 1000084 CAR, 15 flut 20 % 15V 1 58 1103340 BIODE, ZENER, 8,3V 5%, 1W 1 59 1300365 RES IK 1/4W 5% 2 1000084 INSURANCE CAR 15 flut 10					4					
54 9009185 JUMPERS, INSULATED 13 W1-W9,WIO-WI3 55 1909667 IC. 74H74 1 E67 56 1909931 IC. 74H04 1 E32 57 1000084 CAP, 15\$\text{UI}\$ 20\$\tilde{x}\$ 15\$\tilde{y}\$ 1 Fi\$\tilde{\text{O}}\$ 58 1300365 RES IK 1/4W 5% 2, 3 R37,R38 59 1300365 RES IK 1/4W 5% 3, 3 R37,R38 60 1909929 I.C. 74I7 I E43 61 105796 BIOSE IN4004			1		8	1 1	1 i			
1909931 IC. 74H04 1 E32 1000084 CAP, 15\$\phi\text{UF} = 20\% 15\psi					13		1 1 1		W1-W9,WIO- WI3	
1000084 CAR, 15¢Uf. 20% 15V 1	55		1909667	IC. 74H74	1					
58 59 60 61 103340 DIODE, ZENER 6,8V 5% IW 1 Fid R37,R38 1300365 RES IK 1/4W 5% 2 R37,R38 1909929 I.C. 7417 E43	56		1909931	IC. 74H04	1 .				E32	
1300365 RES IK 1/4W 5% 2	57		1000084	CAR, 15¢Uf. 20% 15V					CIDO	
60 61 1909929 1.C. 7417 1 E43 1105796 DIODE IN4004	58			DIODE, ZENER, 6,8V 5% IW	+					
61 1105796 1000E 1N4004 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			9107278-10		- ∧}					
63 1300250 RES 1360 1/4W 5% 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	61		+105796	DIODE 1N4004	╅┿╾					
65 1300271 RSS. 220c 1/4W 5% 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	63		1300250	RES 13/00 1/4W 5%	+				1220	
1661 1:00:01/ 1 NCS 10 1/4W 5% 13	666		1300271 1301317		13				R35, R36, R25	
12 O 1 2 O 1	61		1105796 1000076 1300250	DIODE IN4004 CAP 39uf BES 15/0 1/4W 5% LC 7402	± +				C99	
	lo l									
at the contract $ oldsymbol{v} $. The contract $ oldsymbol{v} $ is the contract $ oldsymbol{v} $. The contract $ oldsymbol{v} $	THIS D	RAWING AND SPECIFICATIONS, H	EREIN, ARE THE PROPER	RTY OF DIGITAL EQUIPMENT TITLE			ASSY	NO.	SIZE CODE NUMBER REV.	4
	CORPO PART A PERMIS	RATION AND SHALL NOT BE REI AS THE BASIS FOR THE MANUFA SION COPYRIGHT (A) 19	PRODUCED OR COPIED OF TENTS OF THE PROPERTY OF SALE OF THE PROPERTY OF THE PRO	R USED IN WHOLE OR IN UT7	1 VIDEO					4
THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF DIGITAL EQUIPMENT. TITLE CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN THIS DRAWING AND SPECIFICATIONS, HEREIN, ARE THE PROPERTY OF DIGITAL EQUIPMENT. TITLE ASSY NO. D-UA-M8658-YA-0 B PL M8658-YA-0 M8658-YA-0	Cremis	40A-16-R276(325)	DRB 125	NT CORPORATION"			SHEE	3 OF 4	INSERTION PARTS LIST DATA BASE REV	الـ

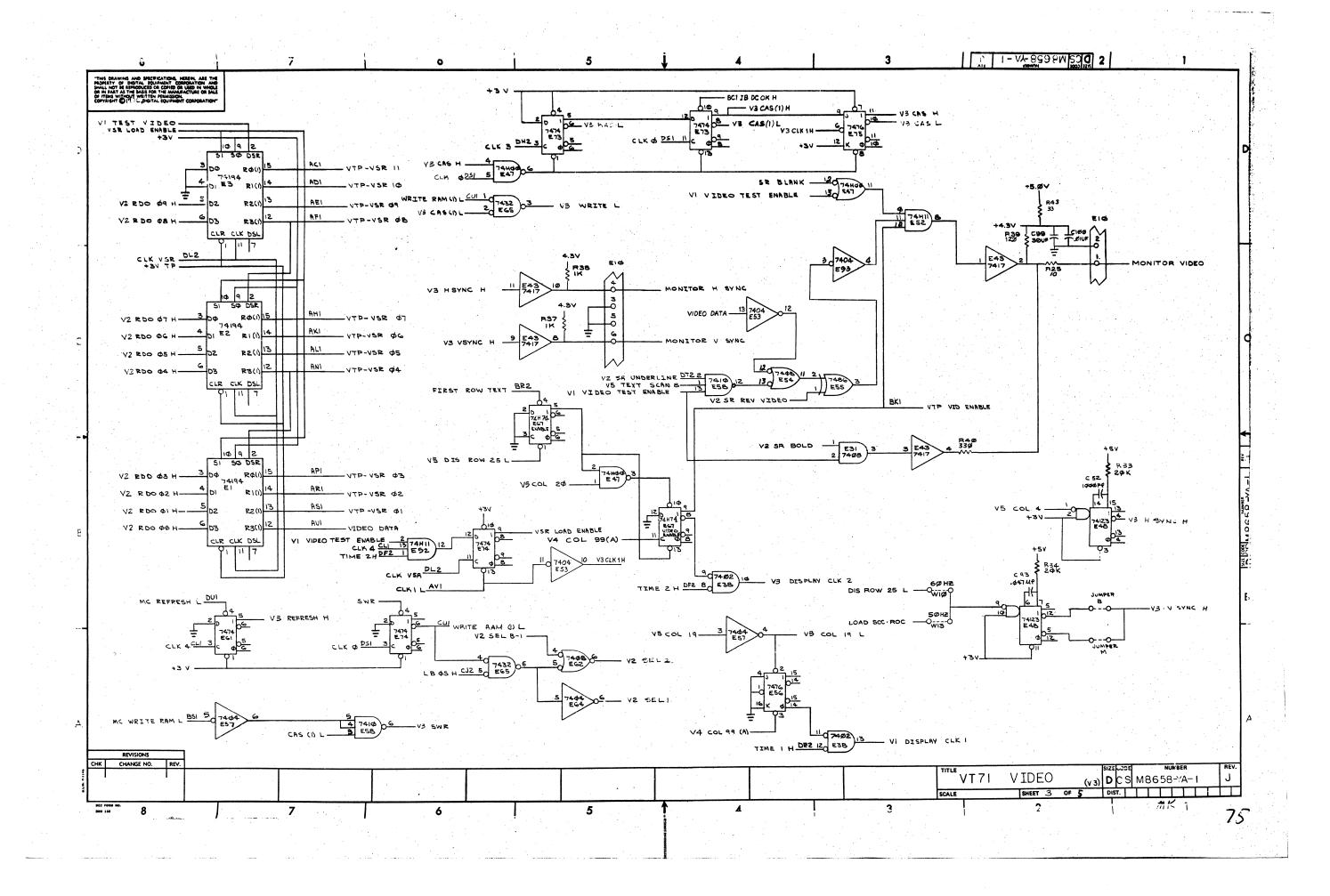
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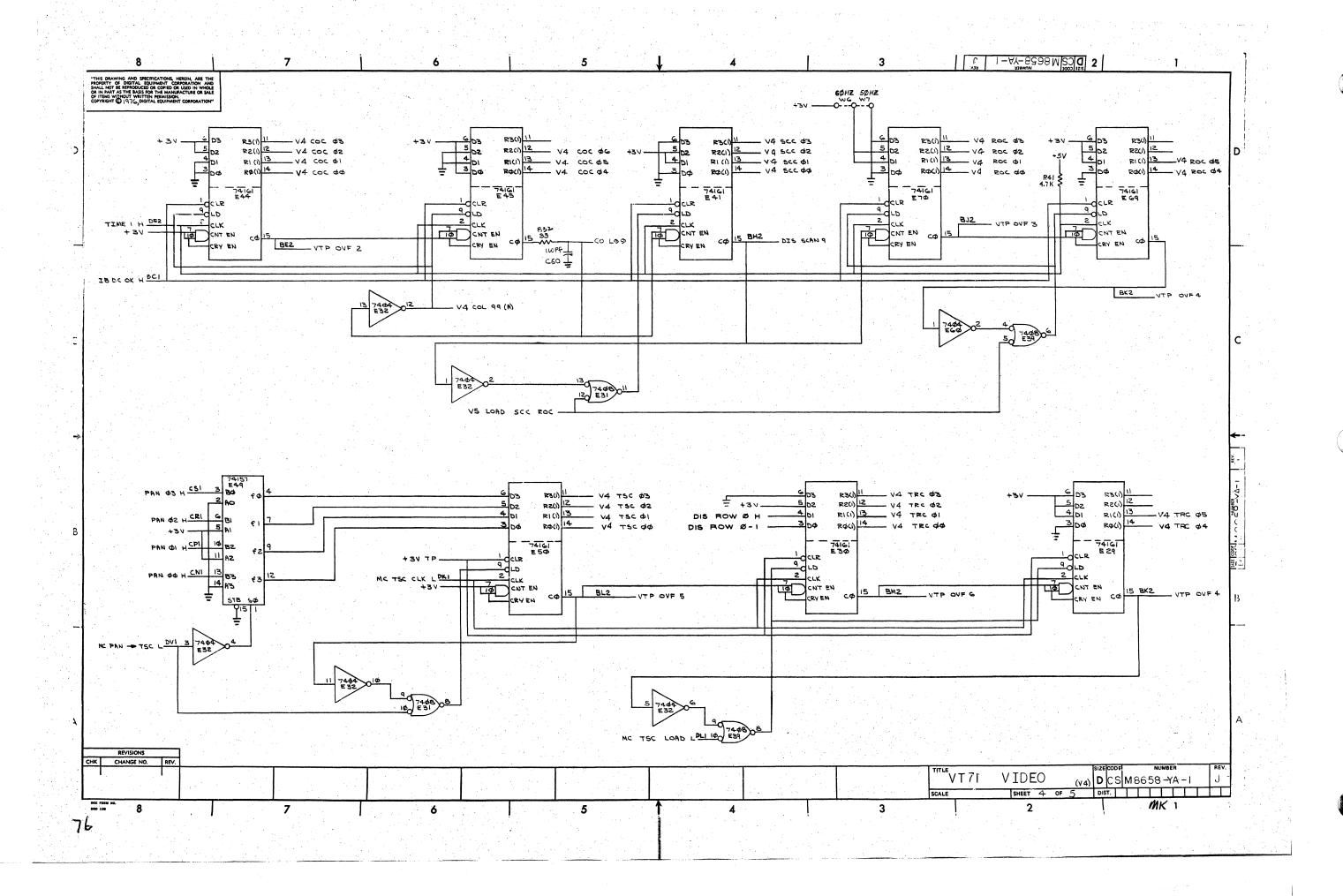


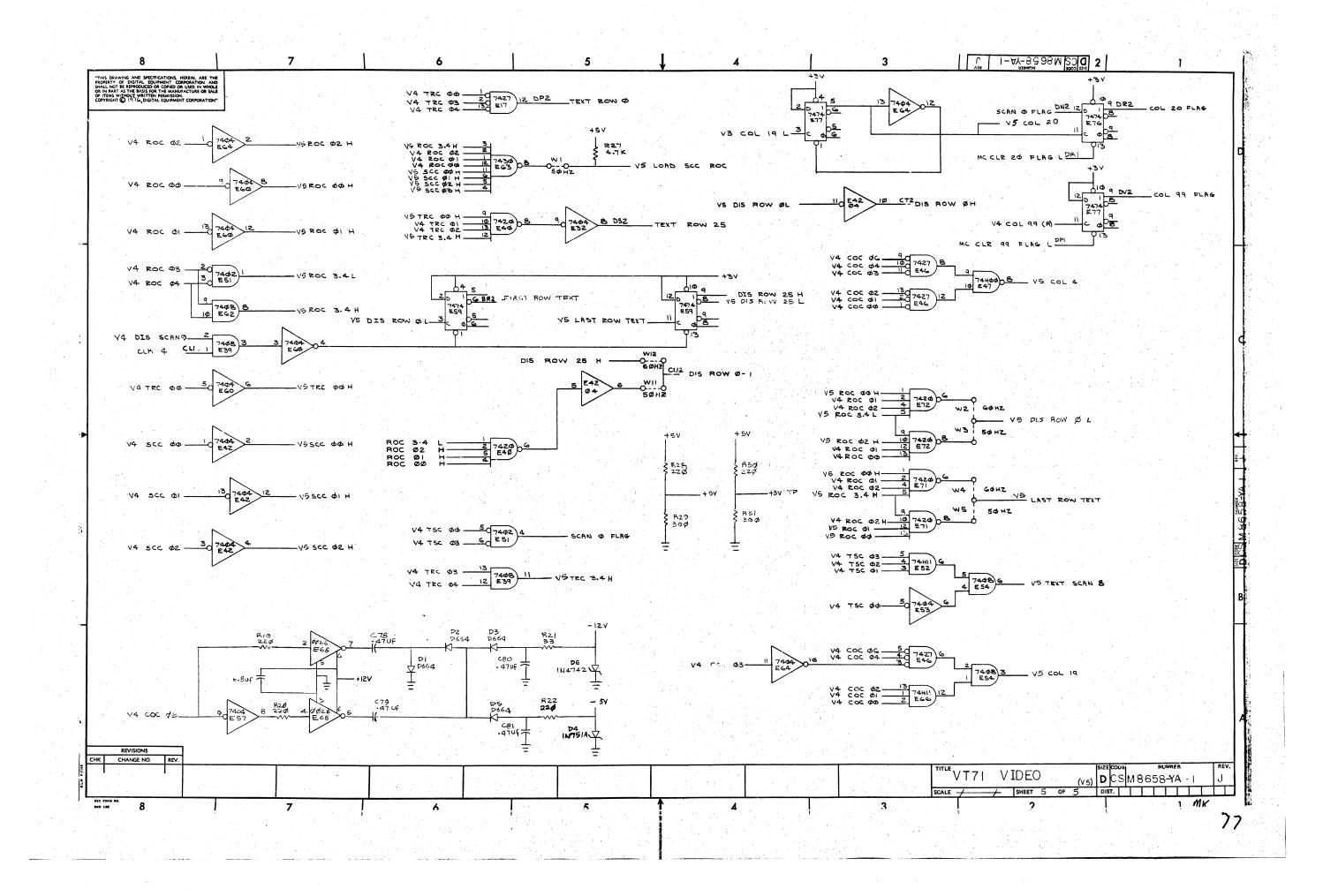


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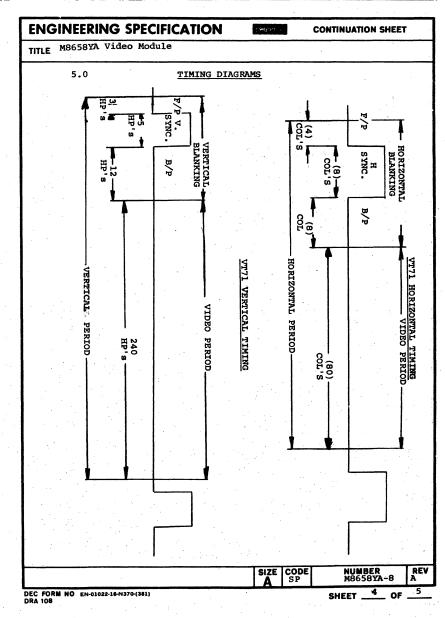
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DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS DATE 2/24/76 FIGURERING SPECIFICATION TITLEM8658YA Video Module REVISIONS REV DESCRIPTION CHG NO ORIG DATE APPD BY DATE 2/24/7 M8658 SPECIFICATION JLW M8658YA SPECIFICATION JLW Don O Com SIZE CODE A SP ENG Dan O Connell NUMBER REV SHEET _1 OF _5

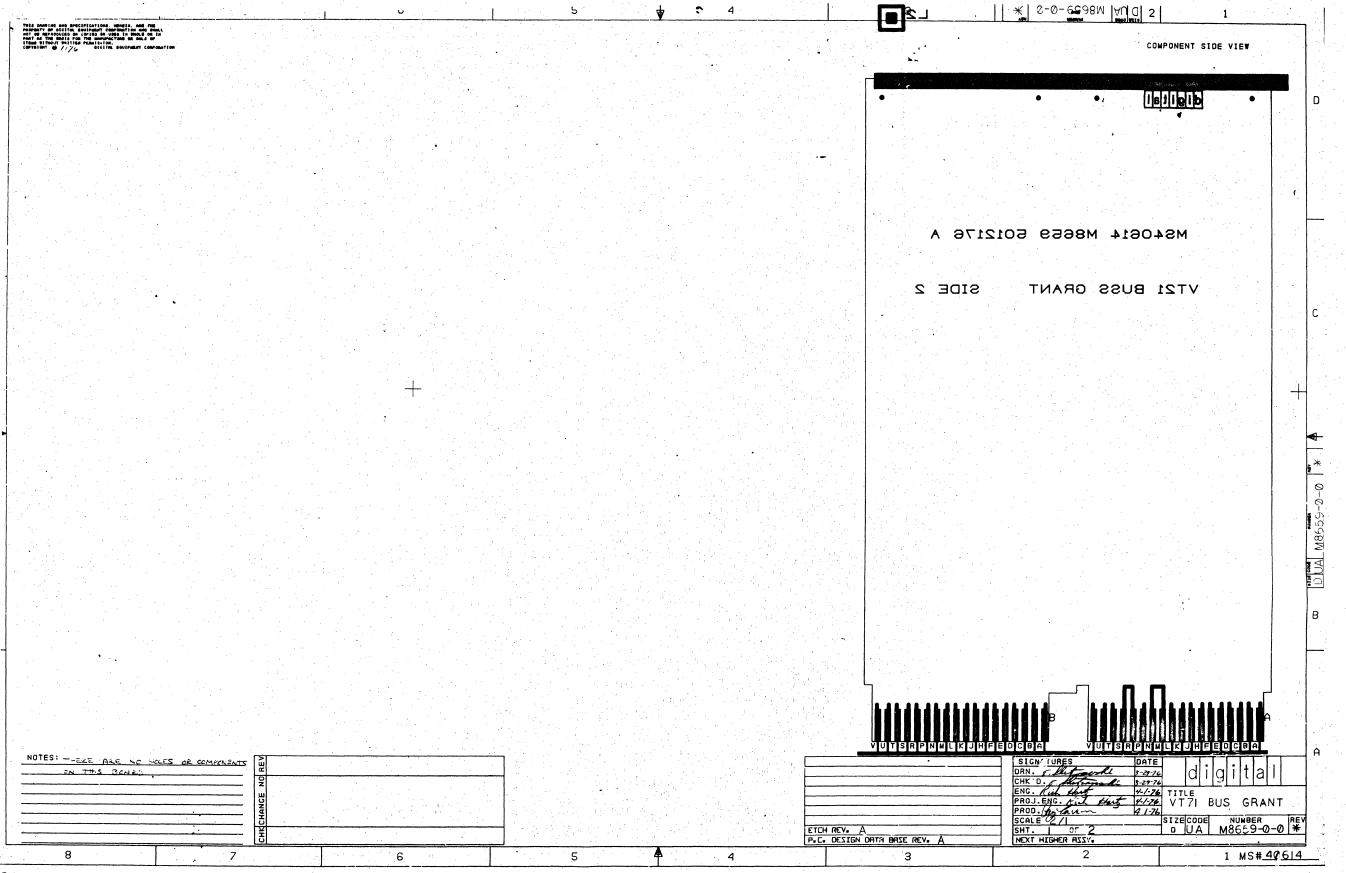
INGINEERING SP	ECIFICA	ATION	digart.		CONTINUATION SHEET	
TLE M8658YA Video	Module					
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VTP OVF 7		COL 20 FLAG			нв Ø3н	CEI
FIRST ROW TEXT		TEXT ROW 25		DS 2		
VTP OVF 1		UNDERLINE		DT2	нв Ø2н	CF1
SP. CHAR. FLAG	CE2	REV. VIDEO		DU2	нв Ø1н	CHl
LB Ø7H	CF2	COL 99 FLAG		DV2	нв ØØн	CKl
LB Ø6H	CH2	VTP 1		AB1	CLK 4	CL1
LB Ø5H	CJ2	VTP VSR 11		AC1	PAN ØØ H	CN1
LB Ø4H		VTP VSR 1Ø		AD1	PAN ØIH	CP1
		VTP VSR Ø9		AE1	PAN Ø2H	CRl
LB Ø3H		VTP VSR Ø8		AF1	PAN Ø3H	CS1
LB Ø2H		VTP VSR Ø7		AH1	WRITE RAM(1) L	CUL
LB Ø1H				AK1	SRL ØØH	CV1
LB ØØH		VTP VSR Ø6		ALI	MC SRL LOBYTE L	DAI
		VTP VSR Ø5				DB1
SPL Ø1H		VTP VSR Ø4	*	ANI	MC SRL CLK	
DIS. ROW ØH		VTP VSR Ø3		APl	MC 40+SRL I	DC1
DIS. ROW 25H	CU2	VTP VSR Ø2		ARL	MC T. VID.OFF L	DD1
Ø FLAG	CV2	VIDEO DATA		AU1	MC CLK RC L	DE1
TIME 1 H	DE2	CLK 1 L		AV1	SRL Ø7(0) L	DF1
TIME 2 H	DF2	IB DCOK H		BC1	MC LOAD SR	DH1
CLK3	DH2	VTP VID. ENA	BLE	BK1	MC TSC CLK	DK1
BLANK		MC WRITE RAM		BS1	MC TSC LOAD	DL1
BOLD		SRL Ø5 H		BU1		DN1
	DL2	+3V TP		BV1		DP1
CLK VSR				CAI		DRI
RC OVF	DM2	нв Ø7н		CB1	CLK Ø	DSI
		нв Ø6н		CCI	MC REFRESH L	DU1
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C FORM NO EN-01022-16-N370-			SIZE	ÇÇP	E NUMBER M8658YA-8	REV

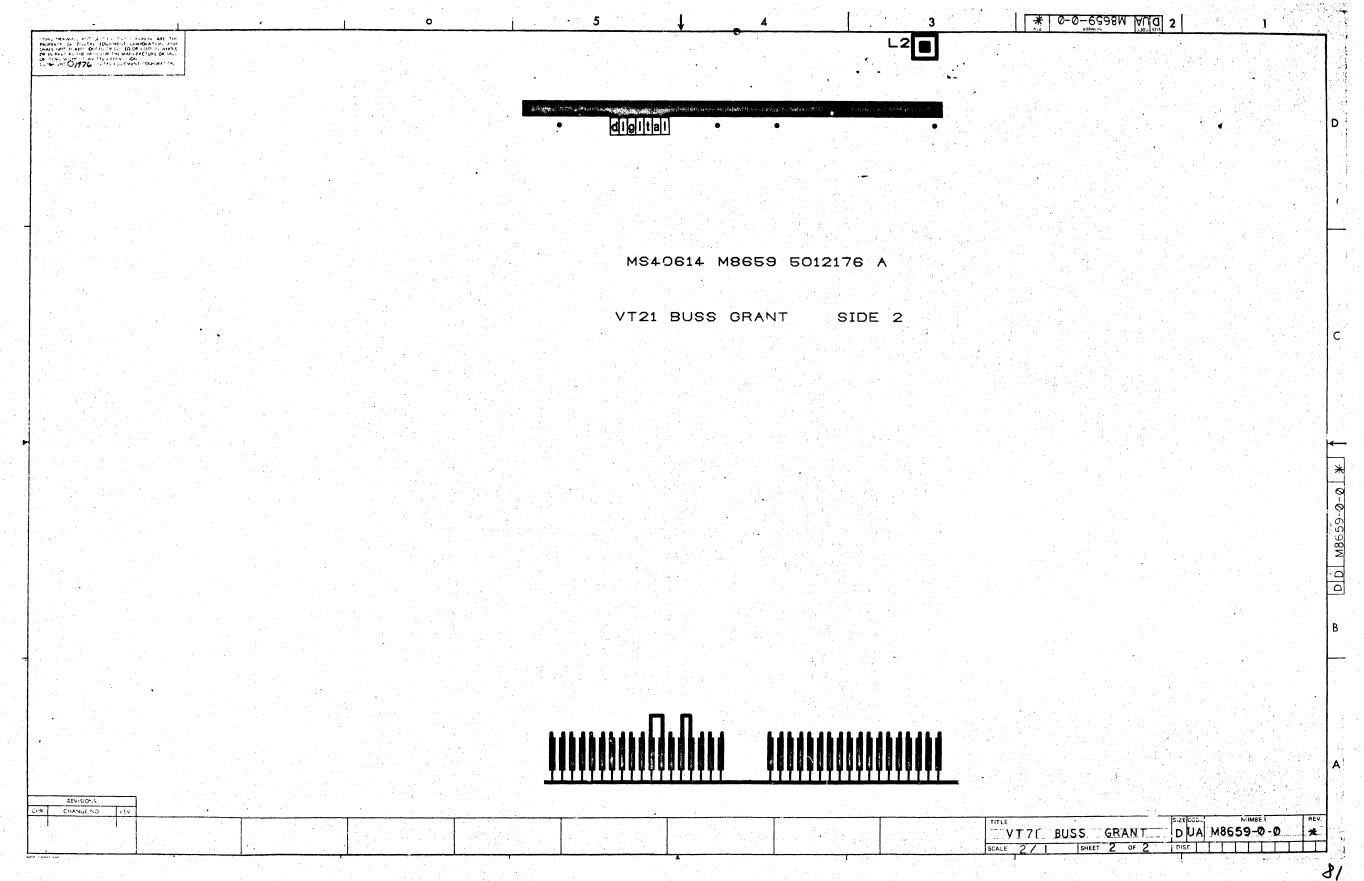
CONTINUATION SHEET TITLE M8658YA Video Module The 8658YA is a video control interface between the VT71 Display Monitor and the M8567YA Control Module. 1.2 The 8658YA receives, from the M8657YA, 16 bits of address and data, control and timing. It transmits all required status information to the M8657YA; it also controls all timing and video data for the VT71 Display Monitor. 1.3 POWER REQUIREMENTS: +5VDC AT 3.2A MAX/2.0A TYP. +12VDC AT 0.6A MAX/0.4A TYP. 2.1 The module has jumper selectable timing for 50 Hz or 60H: it is also jumper selectable for either a Motorola or Ball Brothers Display Monitor. 3.0 JUMPER SELECTION: 60 Hz 50 Hz Motorola 1 = OUT 2 = IN 3 = OUT 4 = IN 5 = OUT 6 = IN 7 = OUT 1 = IN 2 = OUT 3 = IN 4 = OUT 5 = IN 6 = OUT 7 = IN 10 = IN 11 = OUT 12 = IN 13 = OUT 10 = OUT 11 = IN 12 = OUT 13 = IN B = OUT M = IN B = IN M = OUT 4.0 FINGER PINNING: +5VDC AA2 BA2 GND AT1 BC2 BJ1 BM1 VTP RADD ØØ VTP RADD 00 VTP RADD 01 VTP RADD 02 VTP RADD 03 VTP RADD 05 VTP OVF 2 COL 99 AF2 AH2 AJ2 AK2 AL2 BE2 BF2 CA2 DA2 BT1 CC2 CJ1 CM1 CT1 DC2 DJ1 DM1 DT1 AD2 BD2 CD2 +12VDC DIS. SCAN 9 VTP OVF 3 VTP OVF 4 VTP OVF 5 VTP OVF 6 BH2 BJ2 BK2 DD2 AC2 AJ1 AM1 GND BL2 BM2 SIZE CODE NUMBER M8658YA-8 SHEET 2 DEC FORM NO EN-01022-16-N370-(381) DRA 108 OF

ENGINEERING SPECIFICATION



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SOME SHEET		1.	F/P = FRONT PORCH on H SYNC./V SYNC. DELAY.	A-8
		2.	B/P = BACK PORCH on H SCAN /V SCAN DELAY.	NUMBER M8658YA
		3.	HP = HORIZONTAL PERIOD = (64.1 USEC.)	NOW M86
		4.	COL = CHARACTER TIME. = (641 NSEC).	_, ,
3	* -	5.	H SYNC=HORIZONTAL SYNC. SIG. = (5.1 USEC).	
		6.	V SYNC = VERTICAL SYNC. SIG. = (320 USEC).	CODE
	·	7.		
		8.	VERTICAL $B/P = (769.2 \text{ USEC})$	SIZE
		9.	HORIZONTAL $F/P = (2.6 \text{ USEC})$.	
:		10.	VERTICAL F/P 60 HZ. = (192.3 USEC.).	
		11.	VERTICAL F/P 50 Hz. = (192.3 USEC. + 52 HP's = 3.3 MSEC).	
	0	12.	INVERT VSYNC FOR BALL BROS.	
	Module			
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	A Vi			
	M8658YA		그는 이 그림, 네가 되면 화작을 하고 있다. 나는 이번 이번 이번 사람들이 먹고 있는 살으면	
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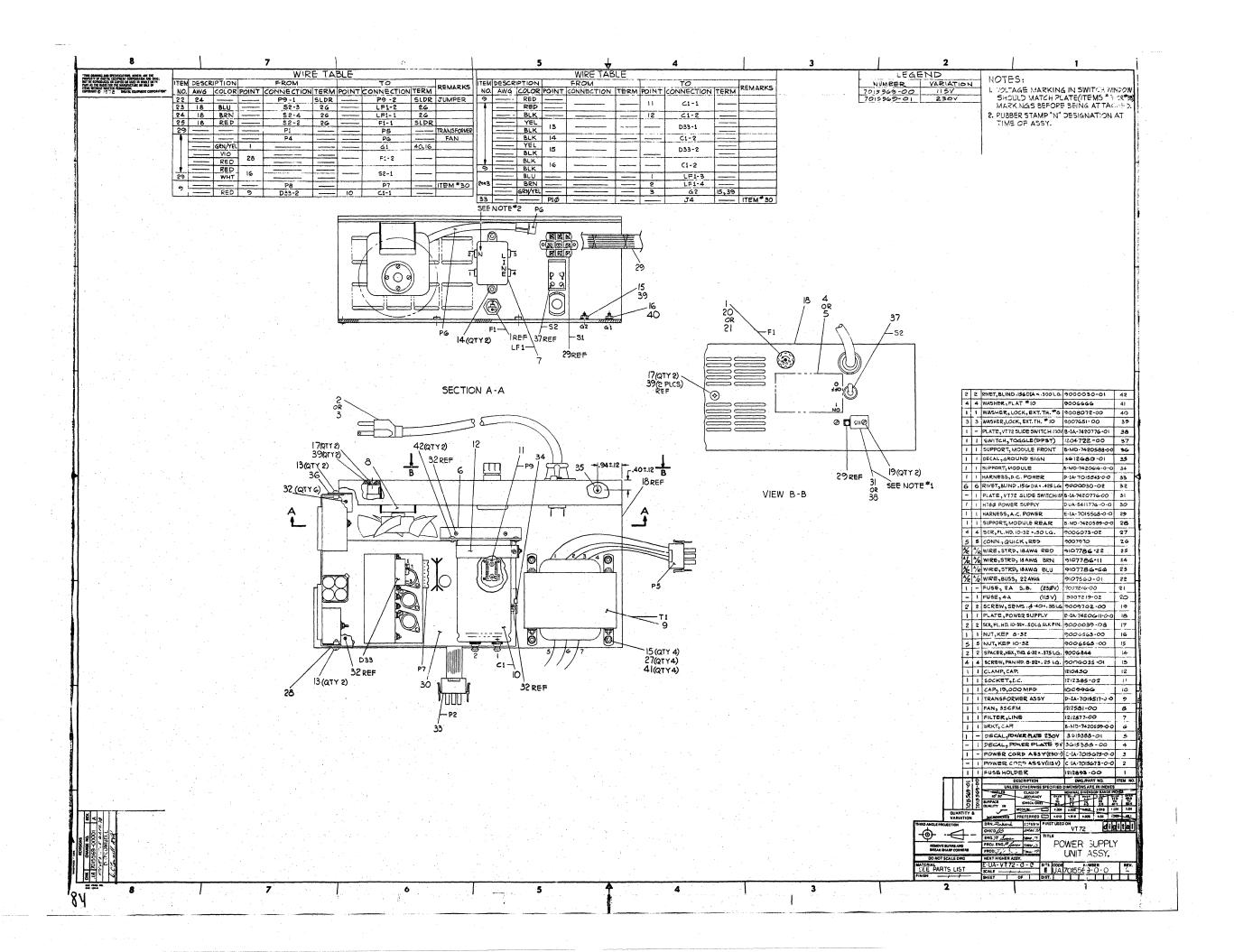
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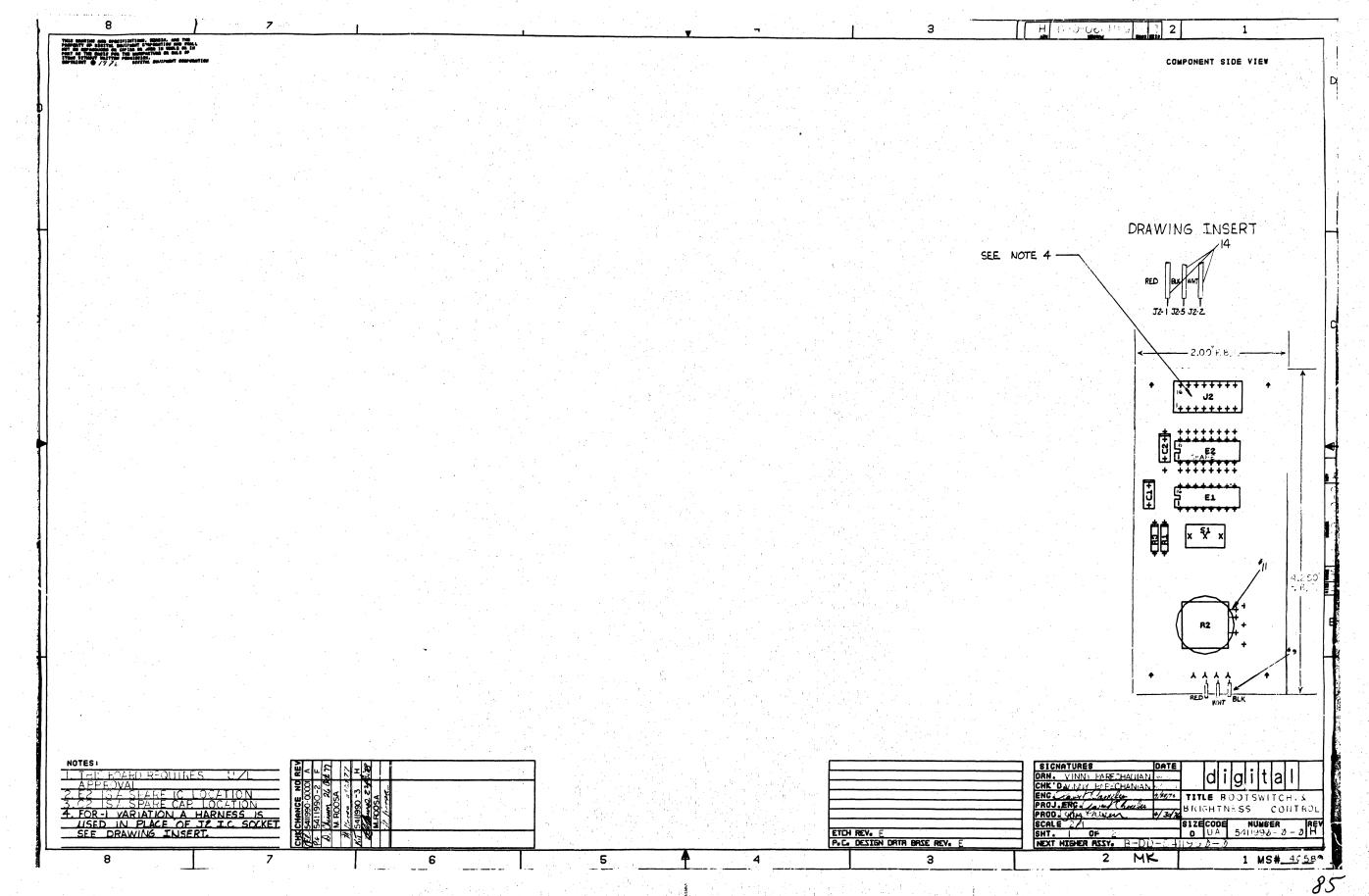
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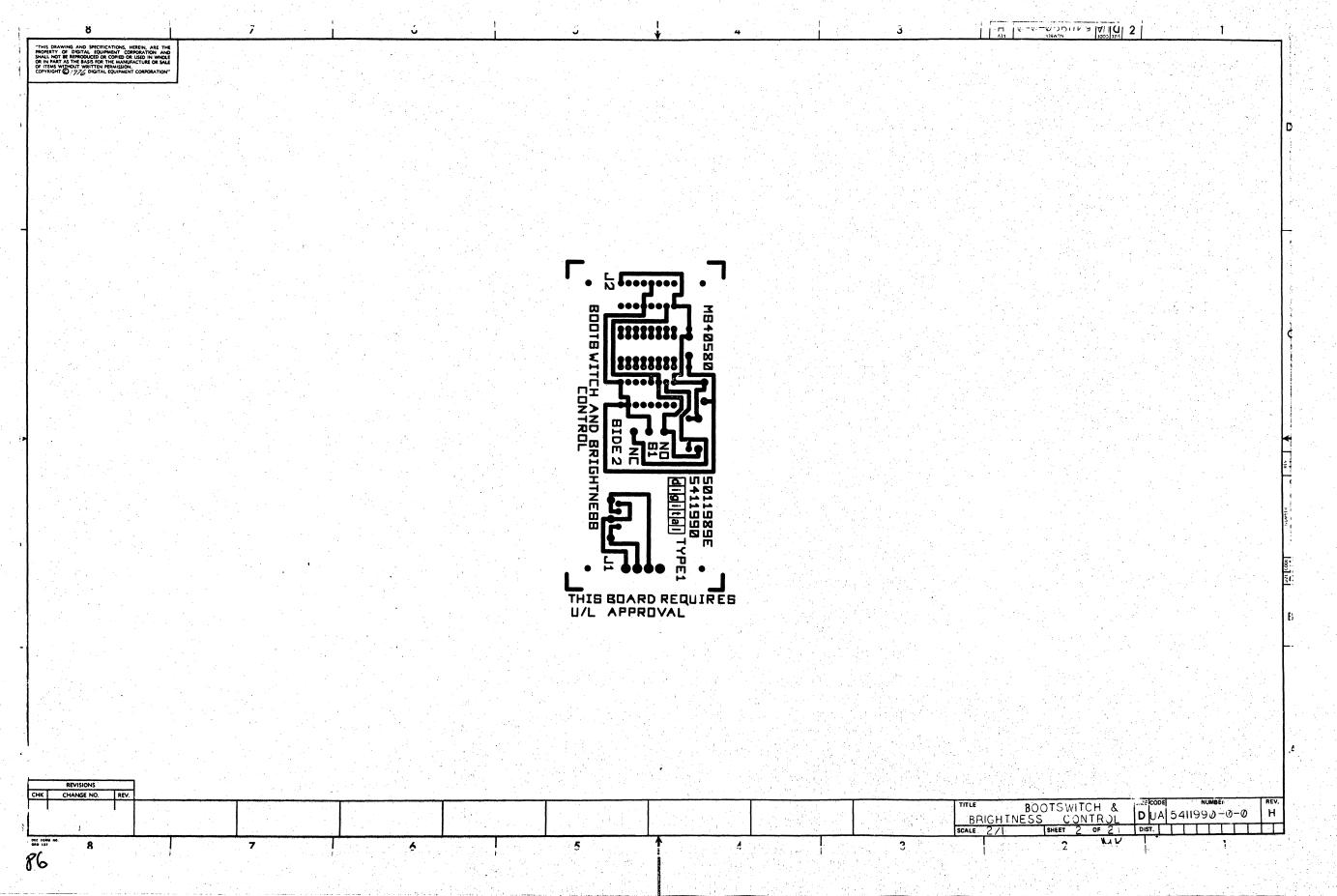
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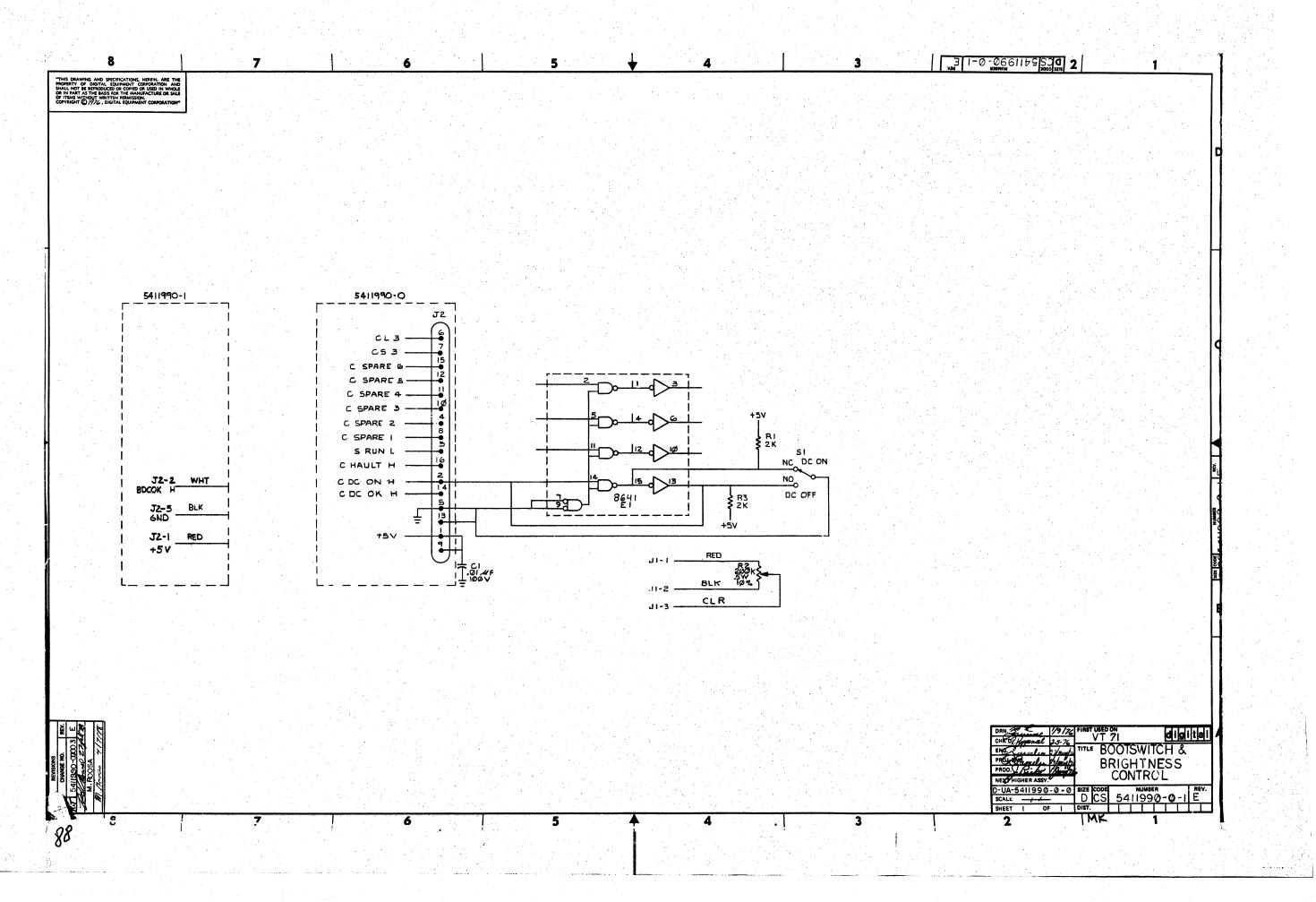
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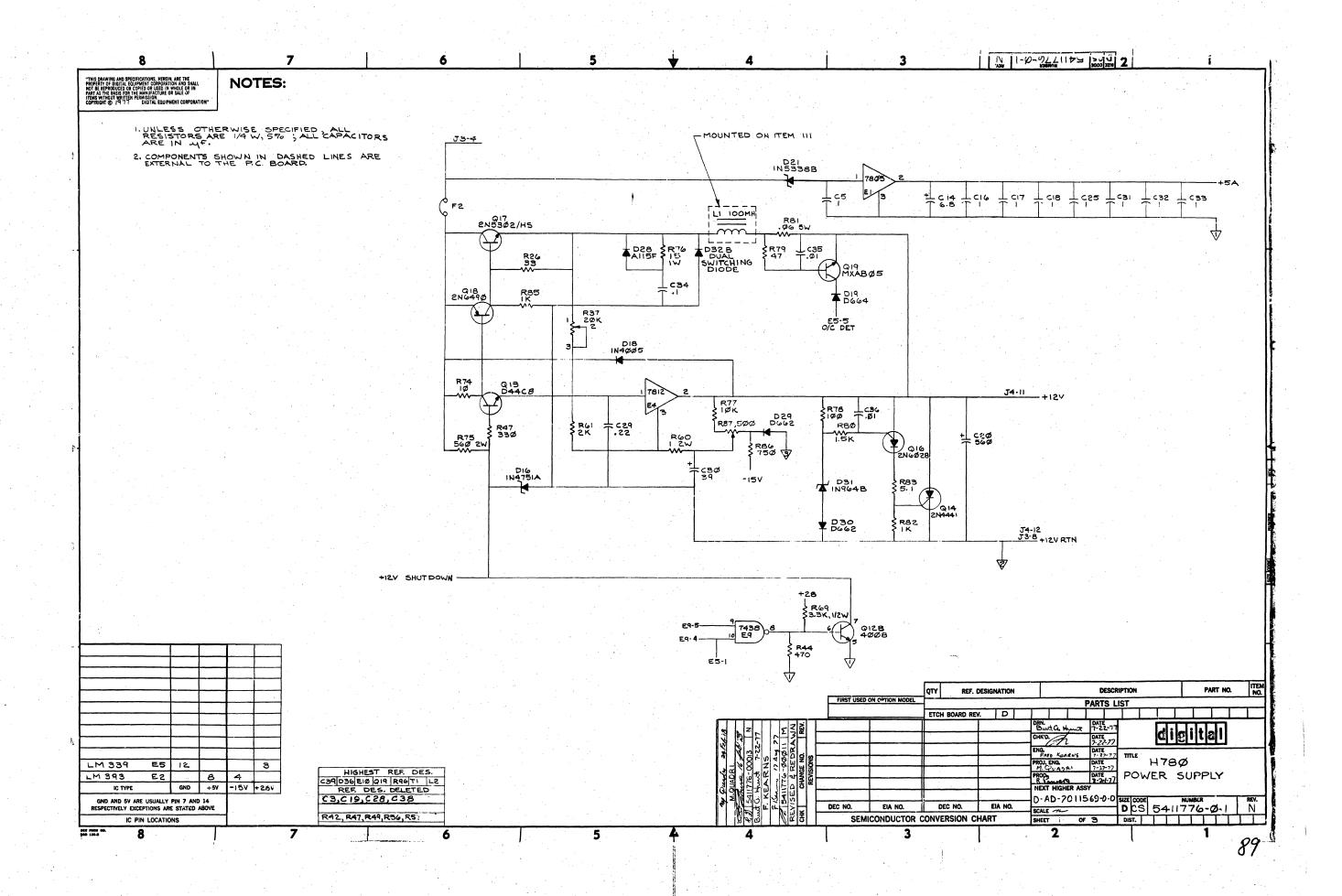
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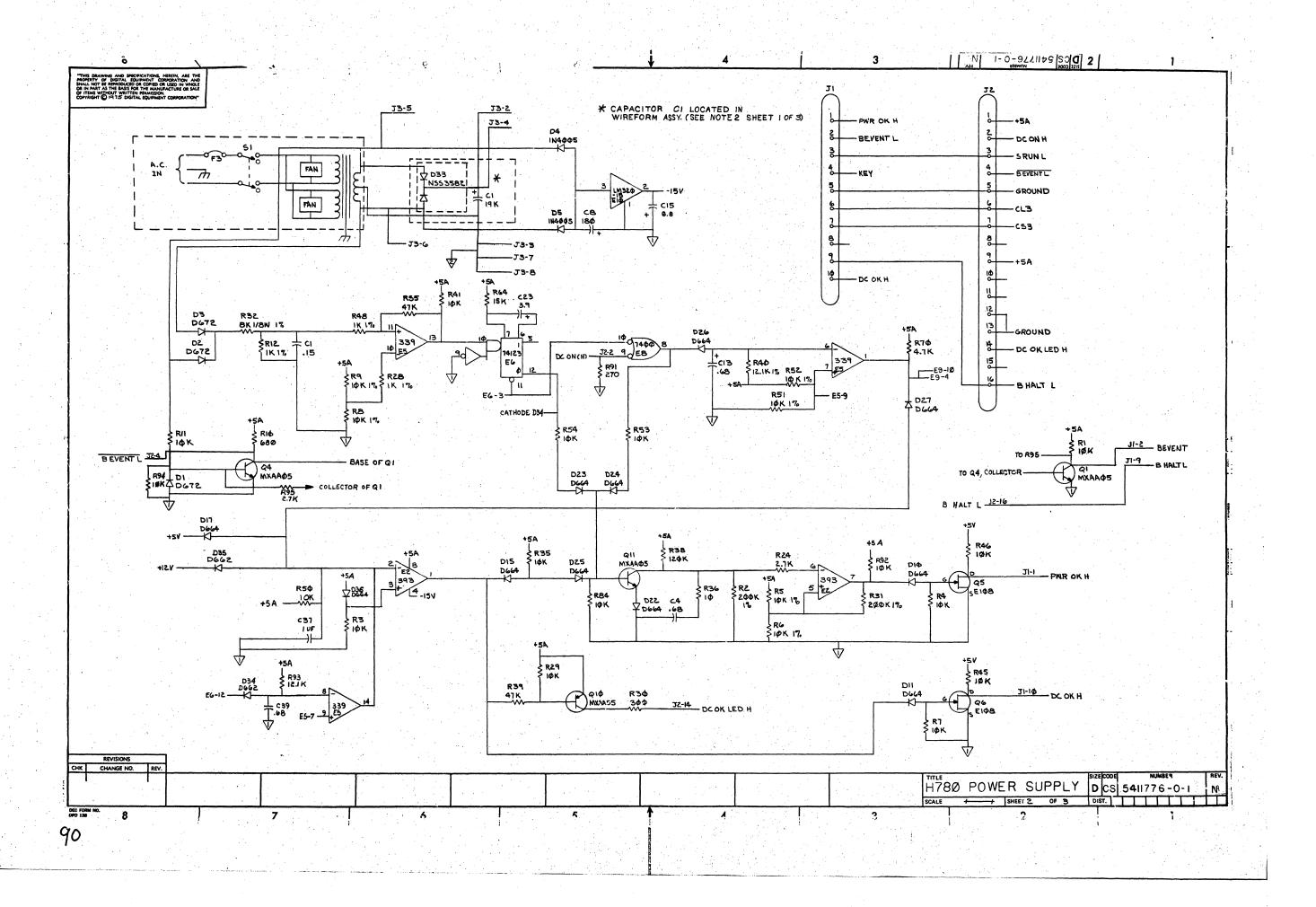
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2	2		1001610-01	.01 MFD 100V OR 50V Z5U DISC/800FF MIN	1	C1 -	
3	3		1210786-01	KNOB, FLASTIC FOR 8A	1		
4	4		1210841-00	SW, TOG SPECIAL SNAP IN VERSION	1	S1	
5	5		1211813-00	SOCKET 16PIN LOW PROFILE	1	J2	
6	6		1302388-00	2 K 1/4W 5% CC (13-00	2	R1,R3	
7	7		1312956-00	200 K .5W 10% FOT	1	R2	
8	. 8		1911579-00	8641 TRANSCEIVER, BUS, QUAD, UNIBUS	1	E1	
9	9	C-IA-7012359-0-0		HARNESS, BRIGHTNESS POT	1		
10	10		9009507-00	****** THIS ITEM IS NOT USED ******	0		
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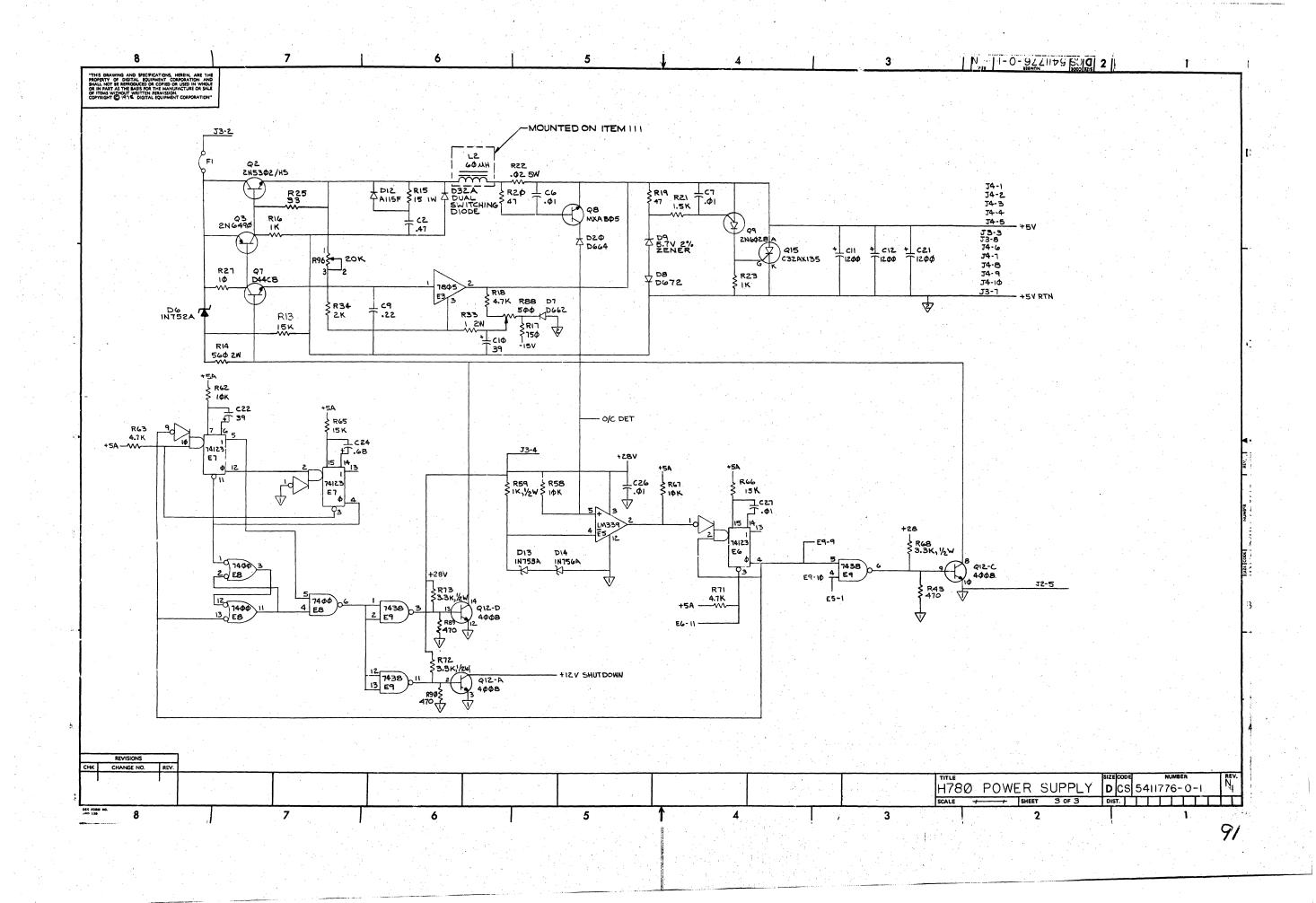
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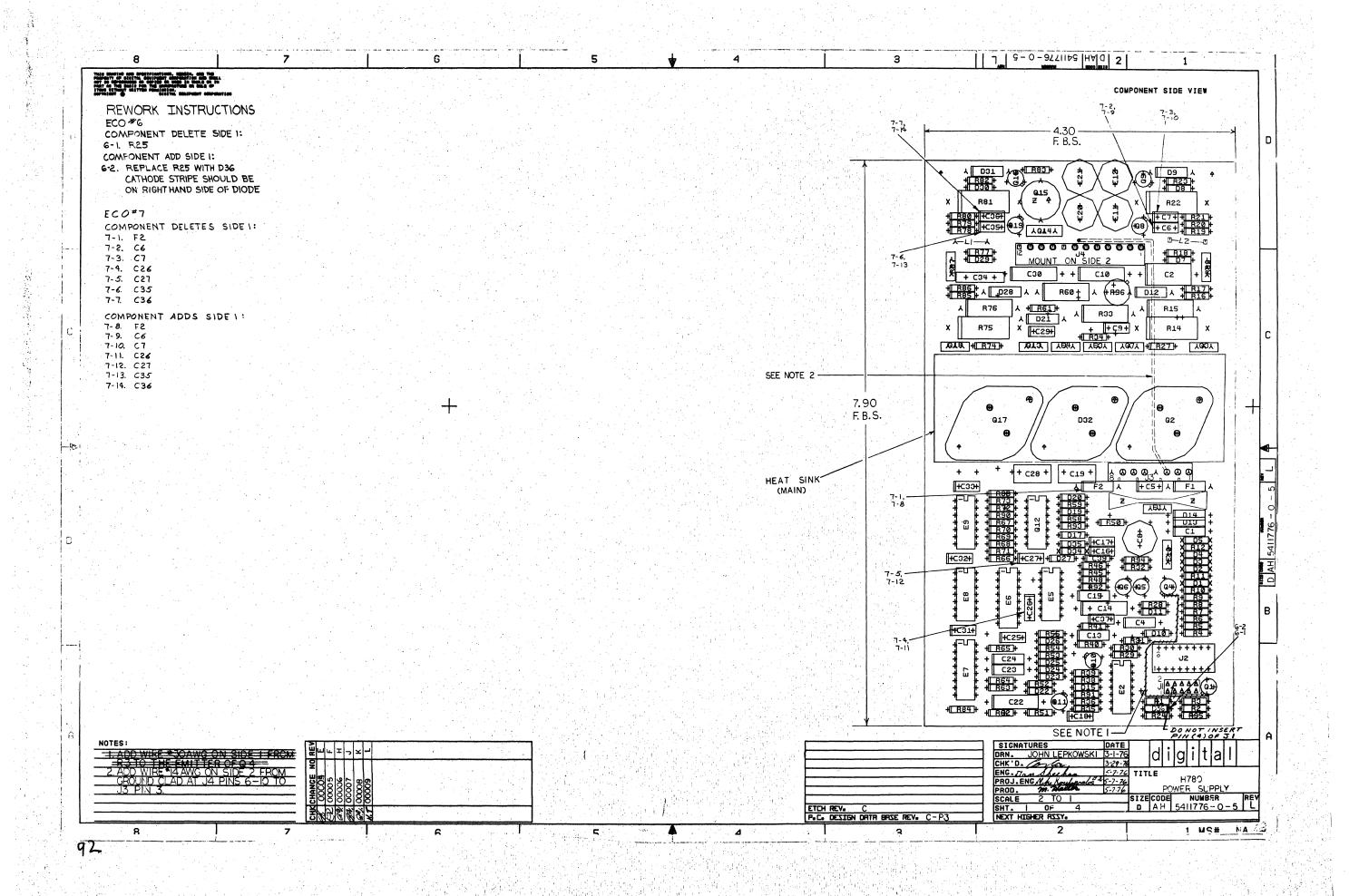


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DRN. JOHN LEPKOWSKI 3-1-76

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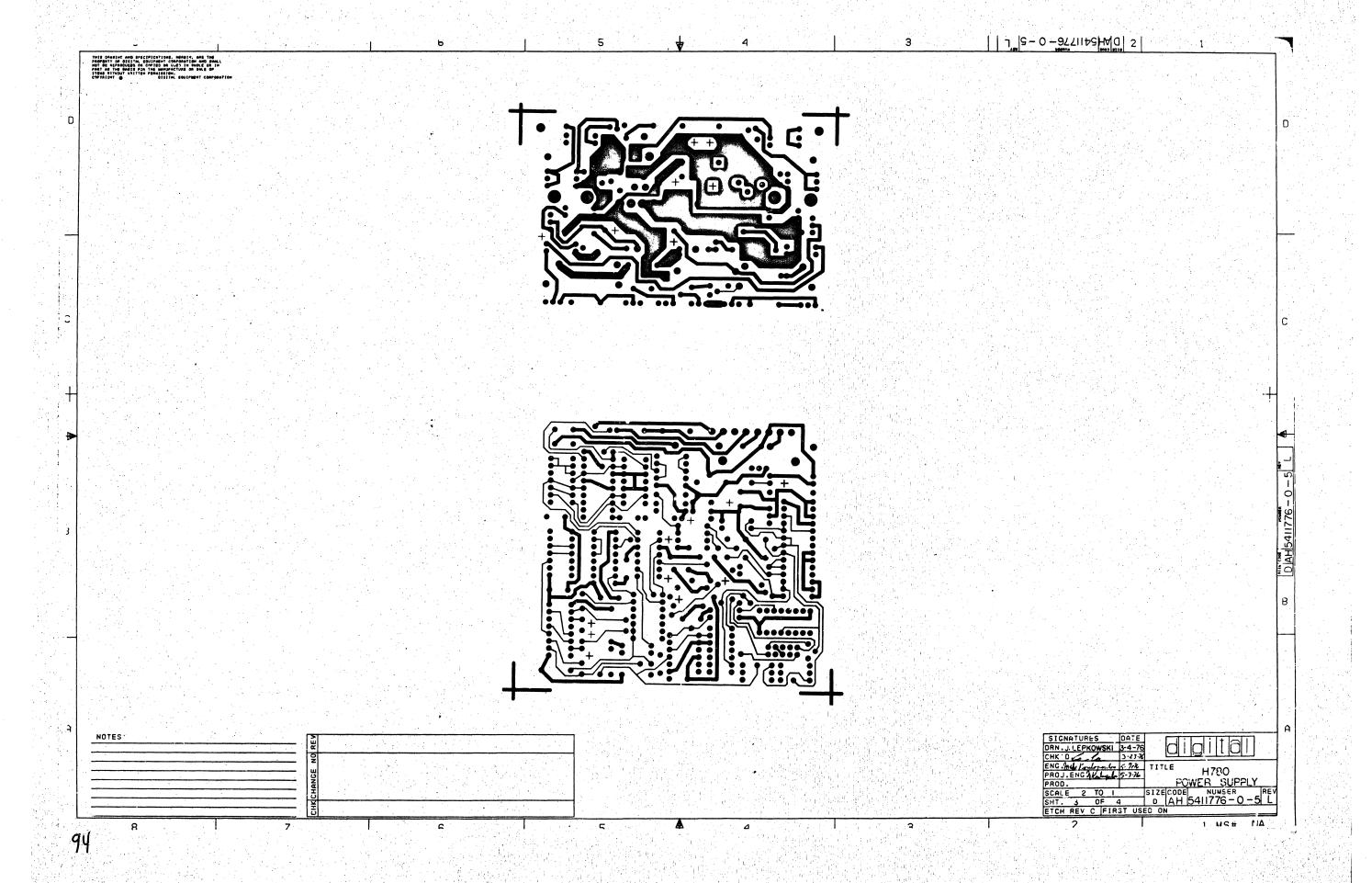
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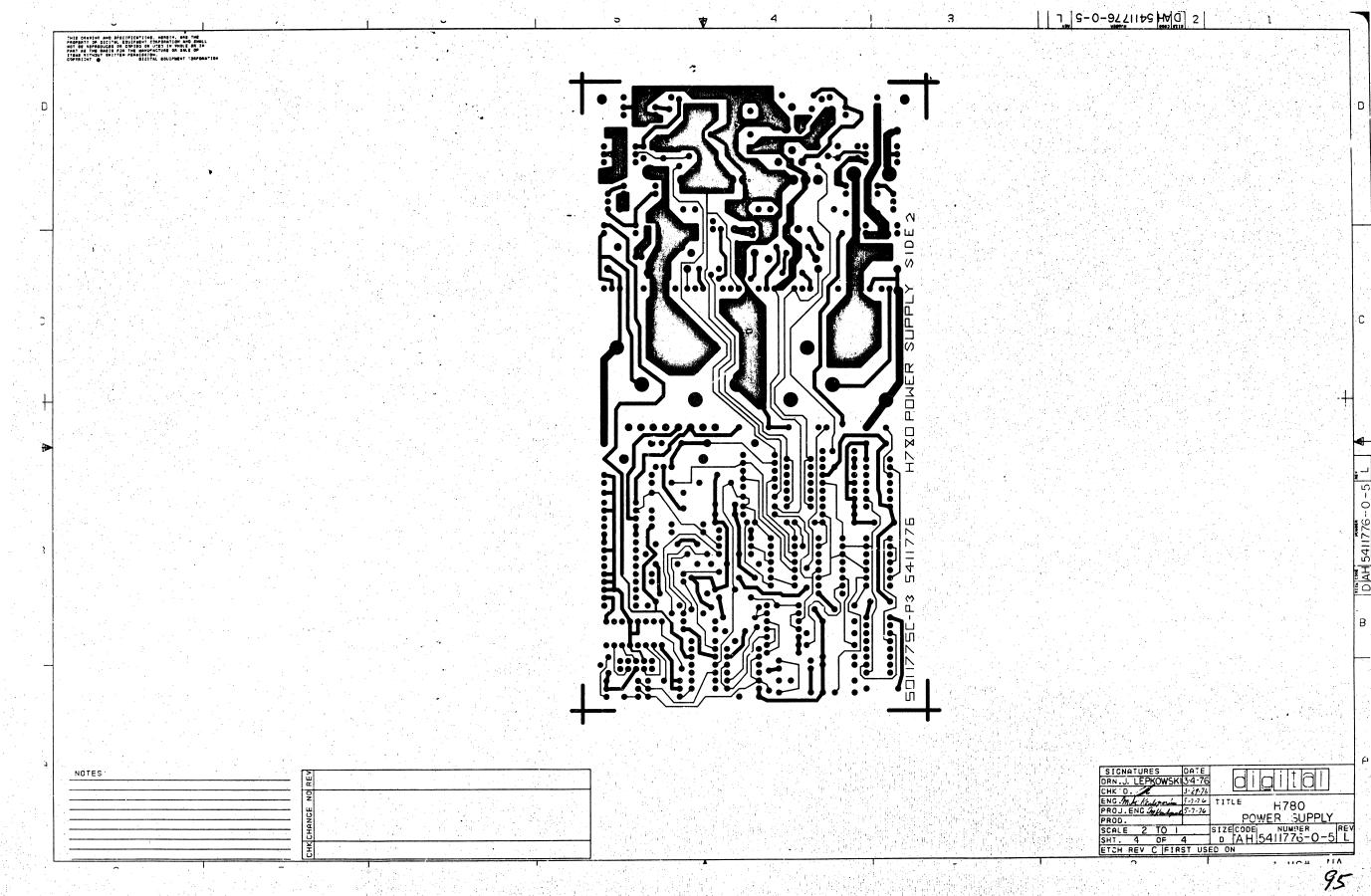
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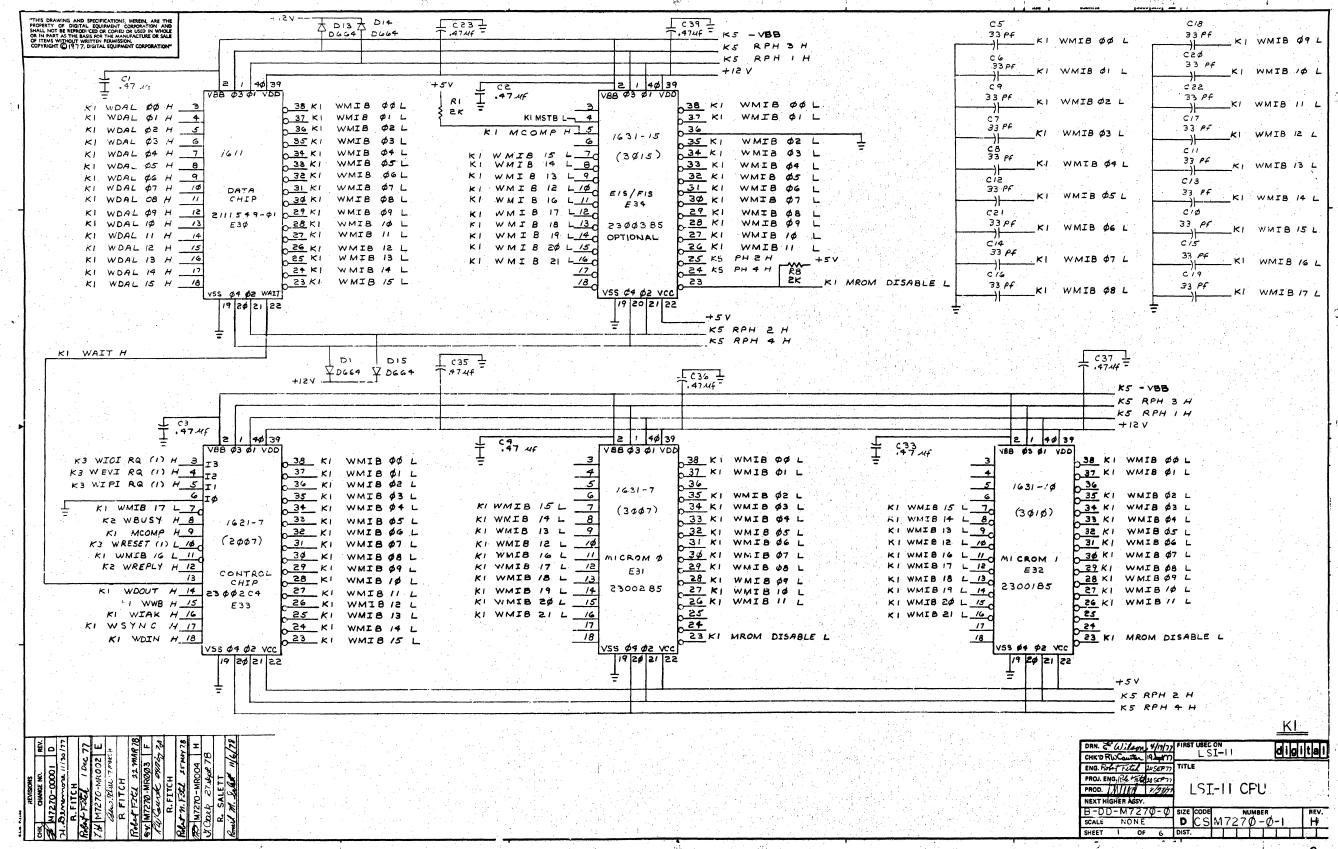


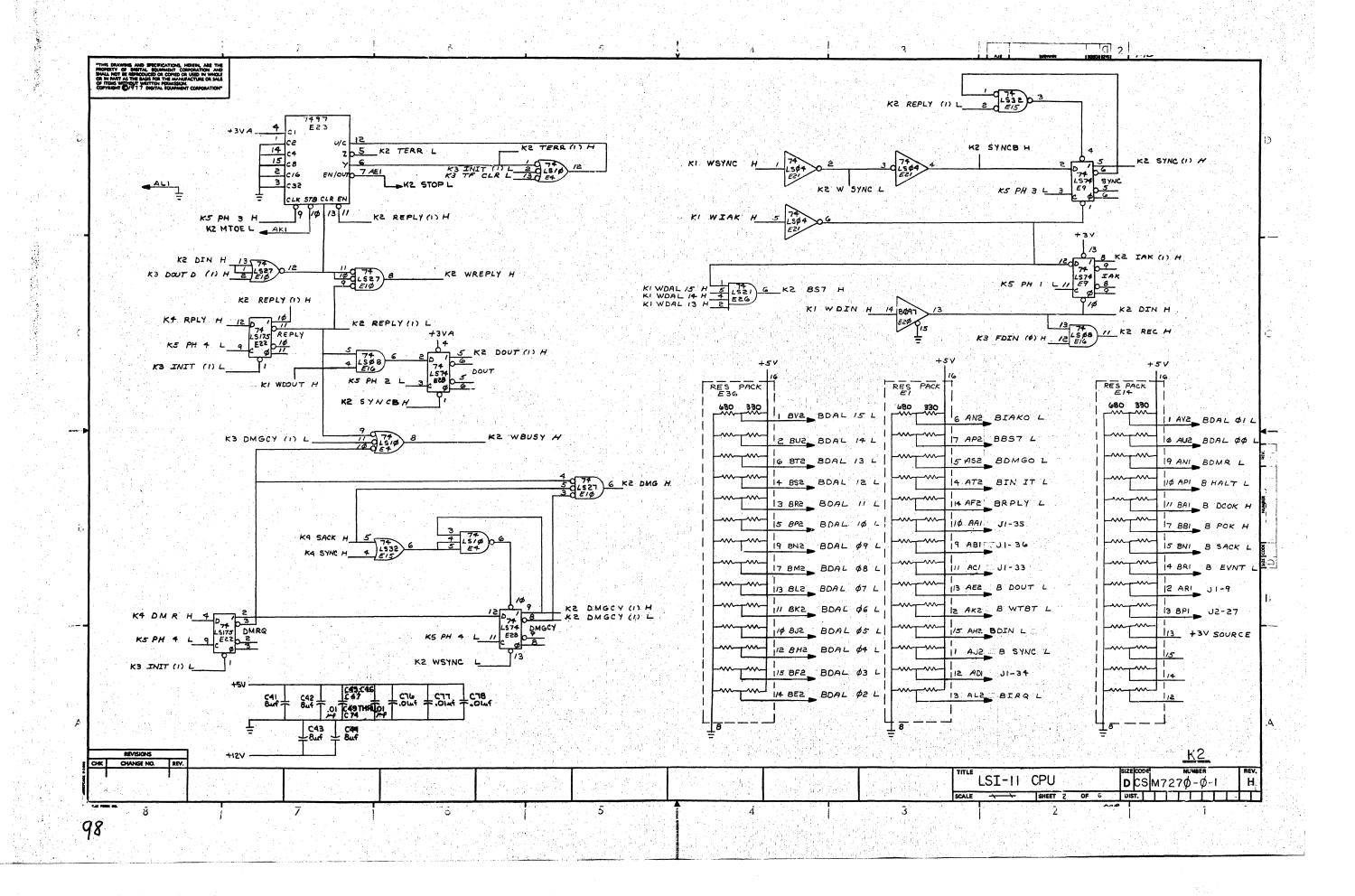
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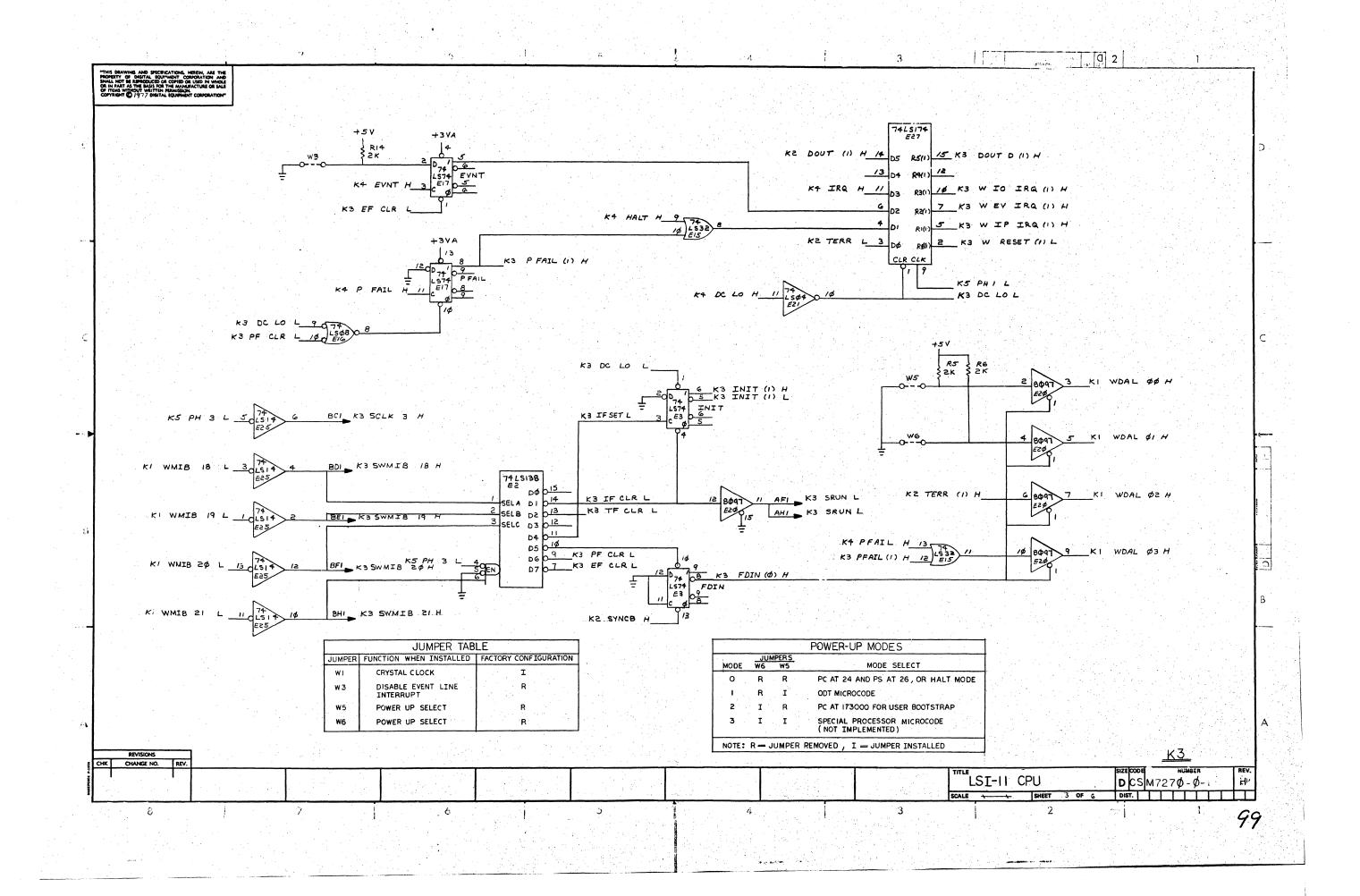
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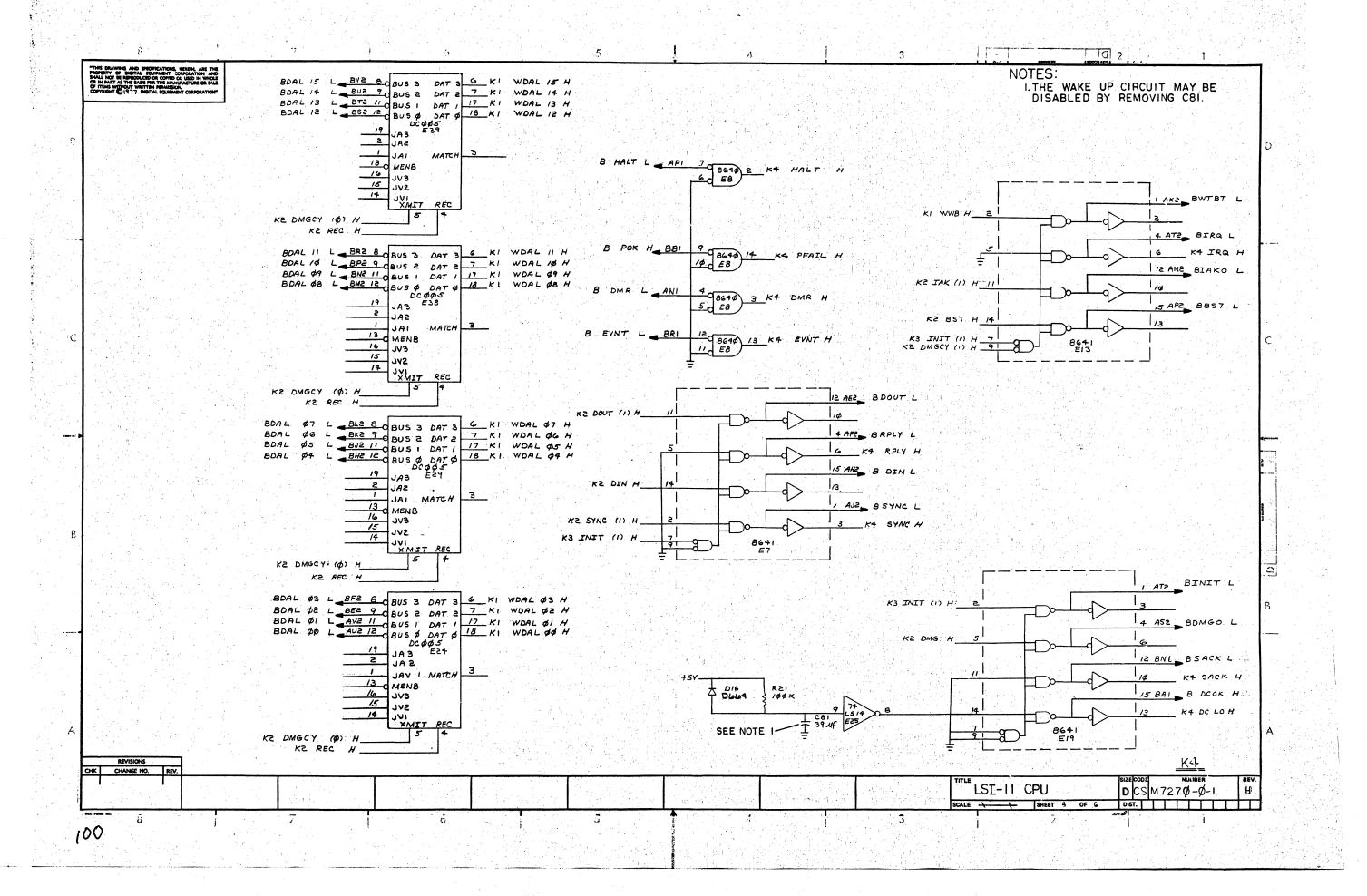


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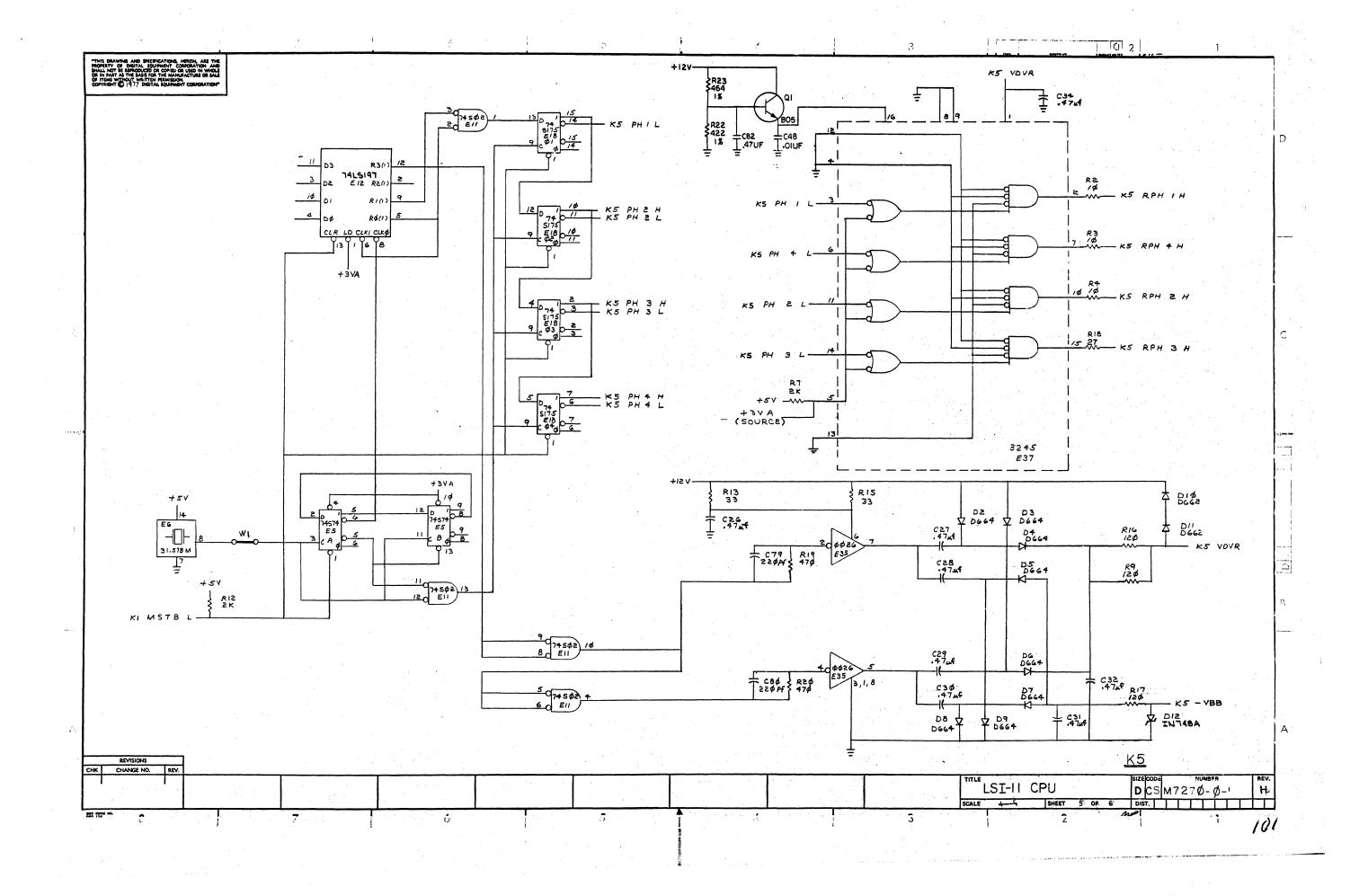


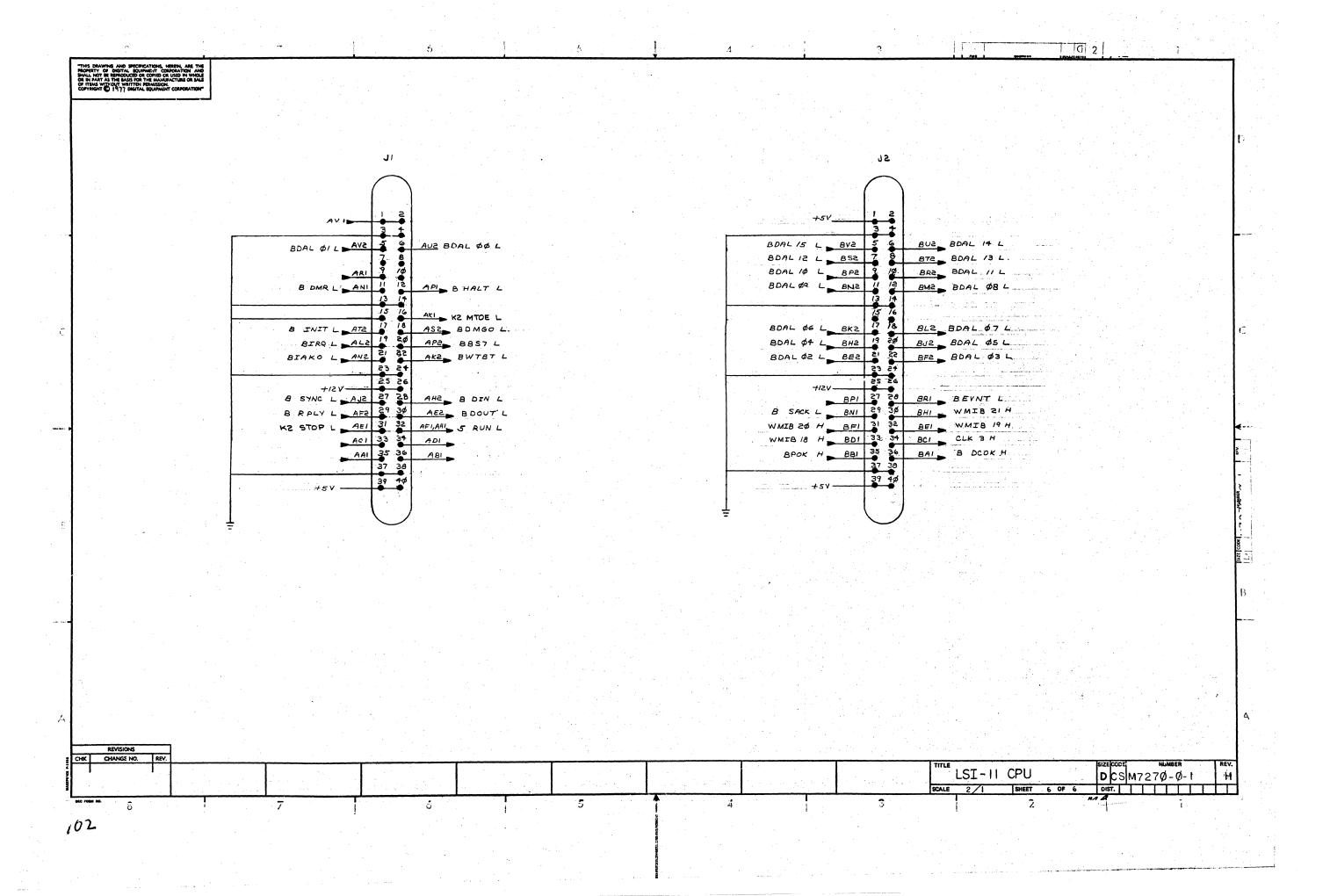


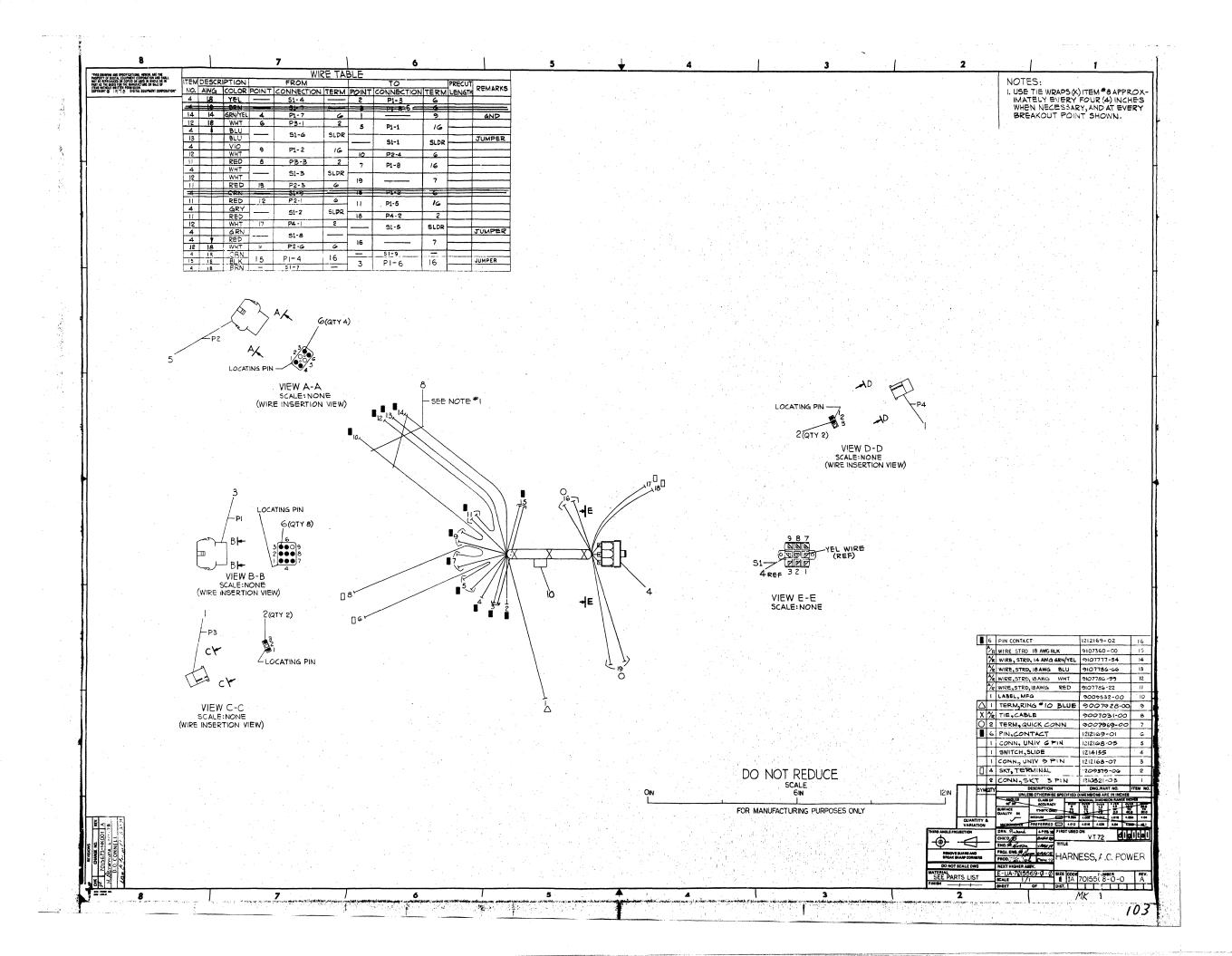


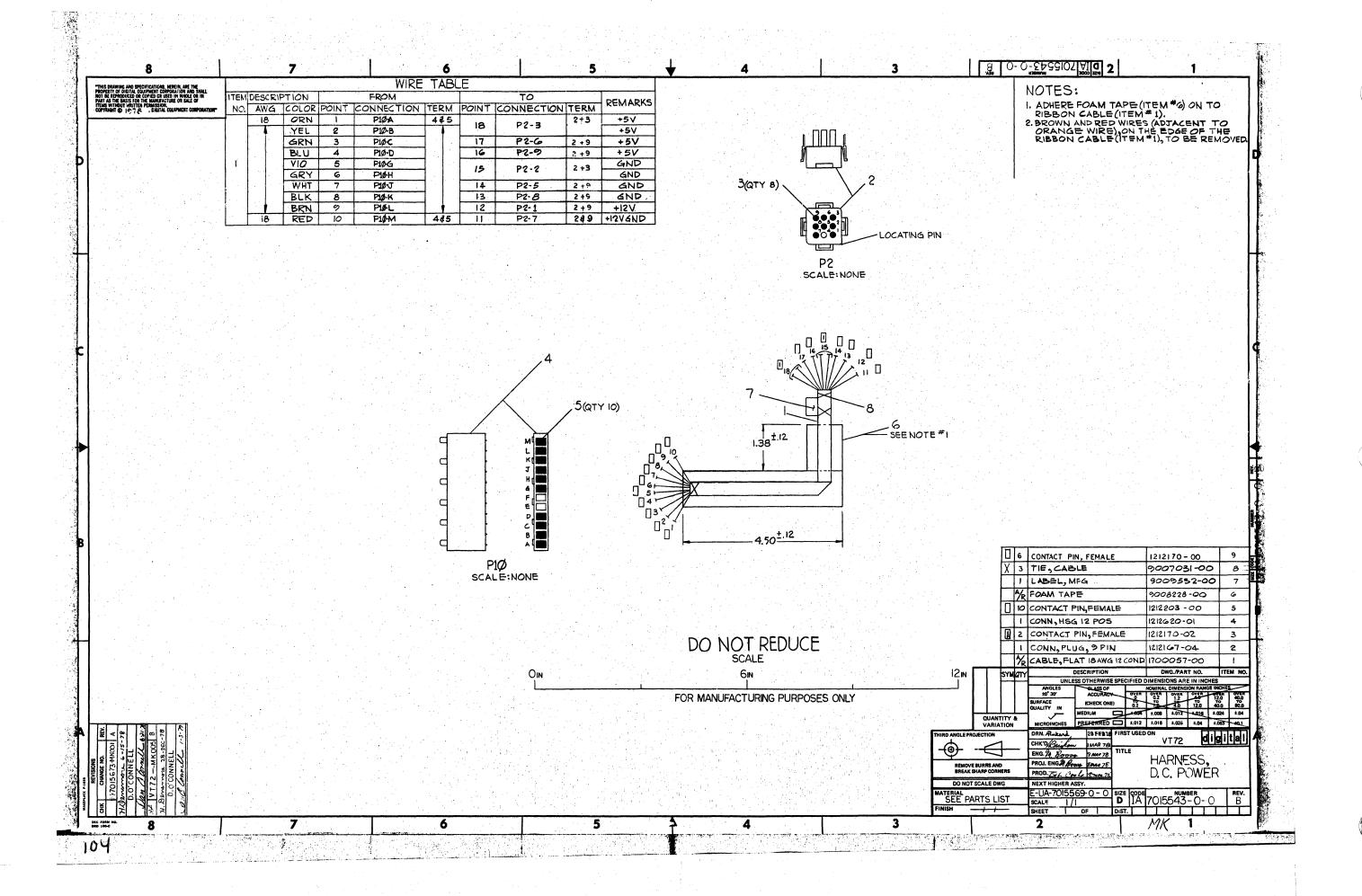
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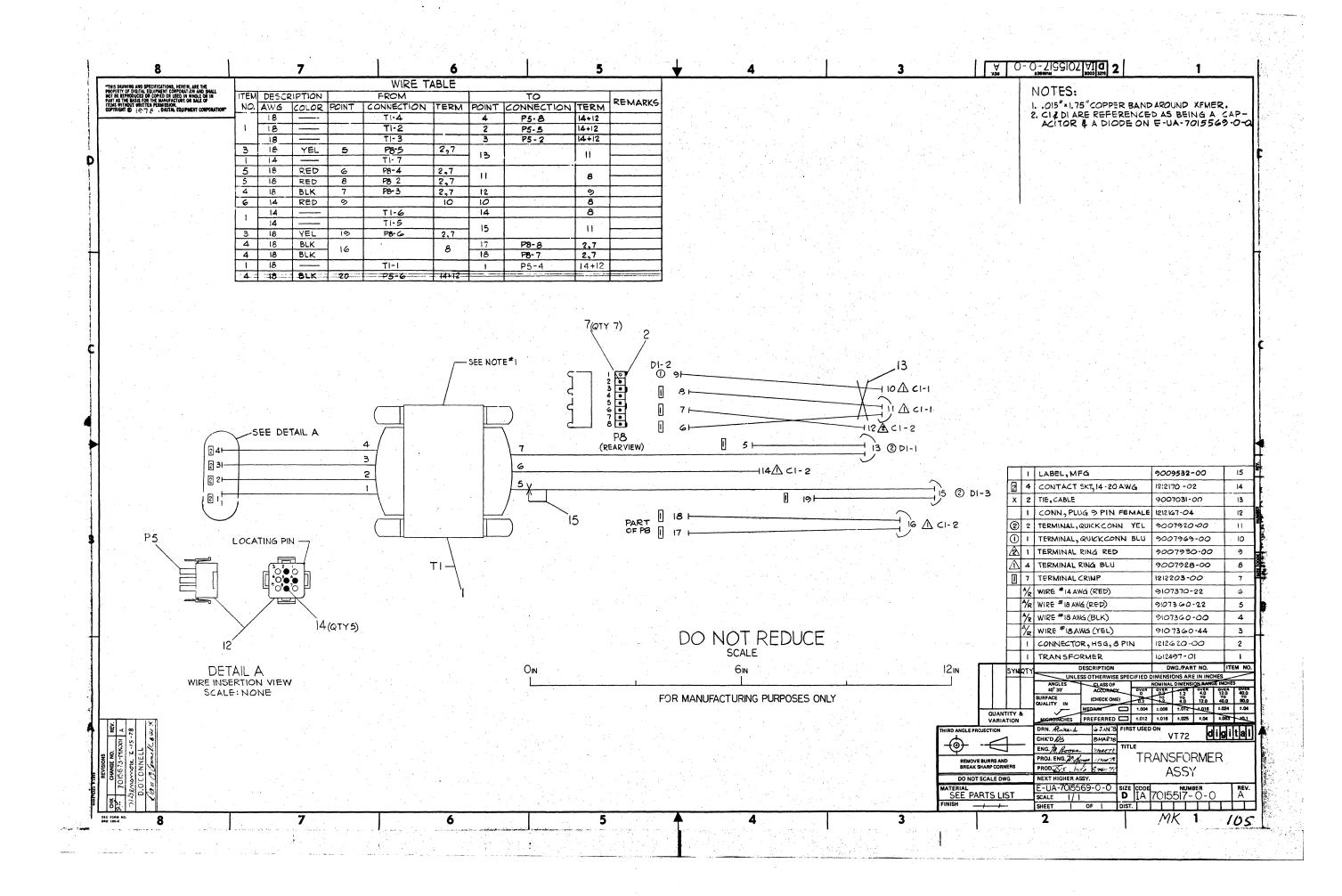
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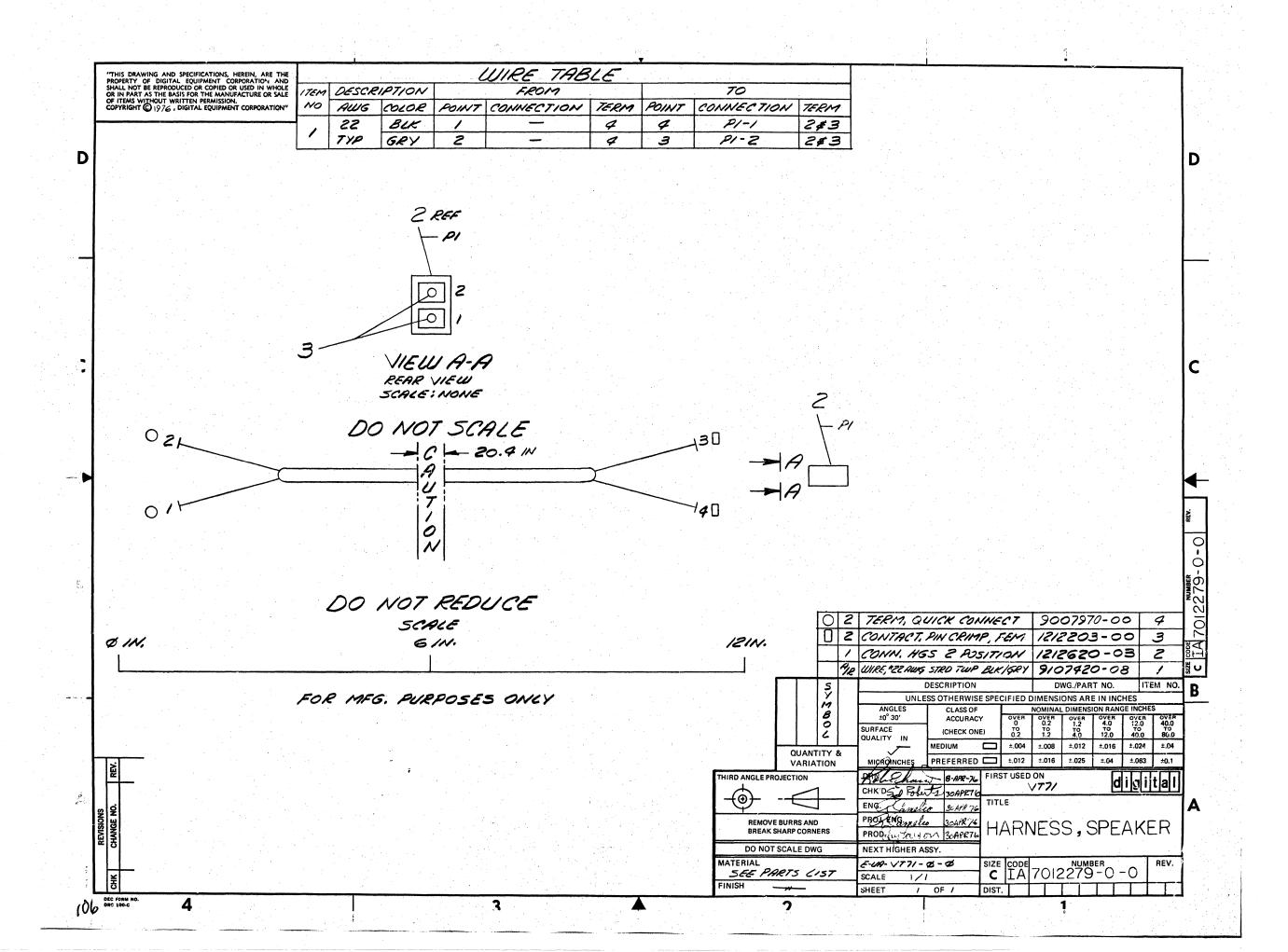


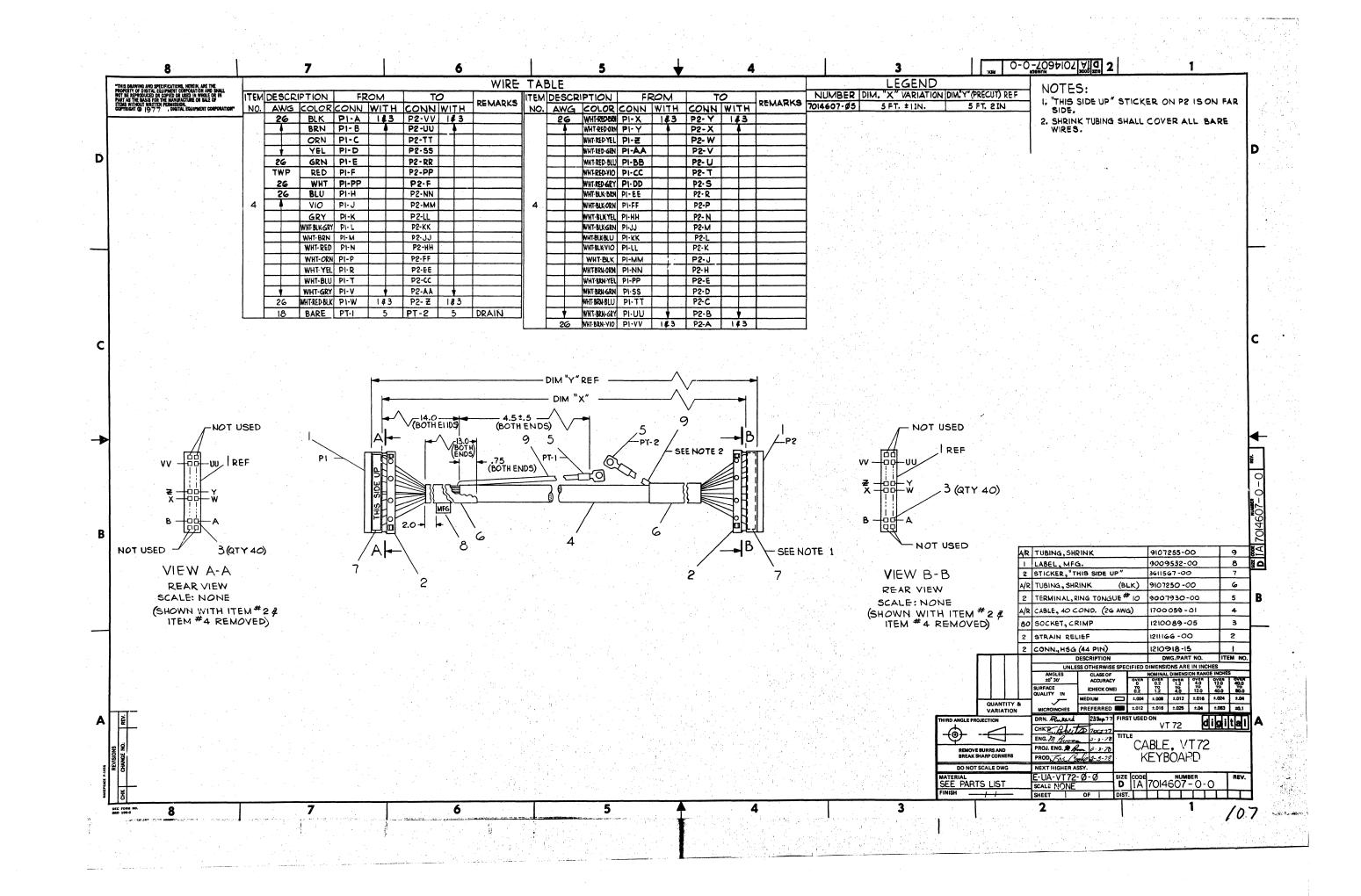


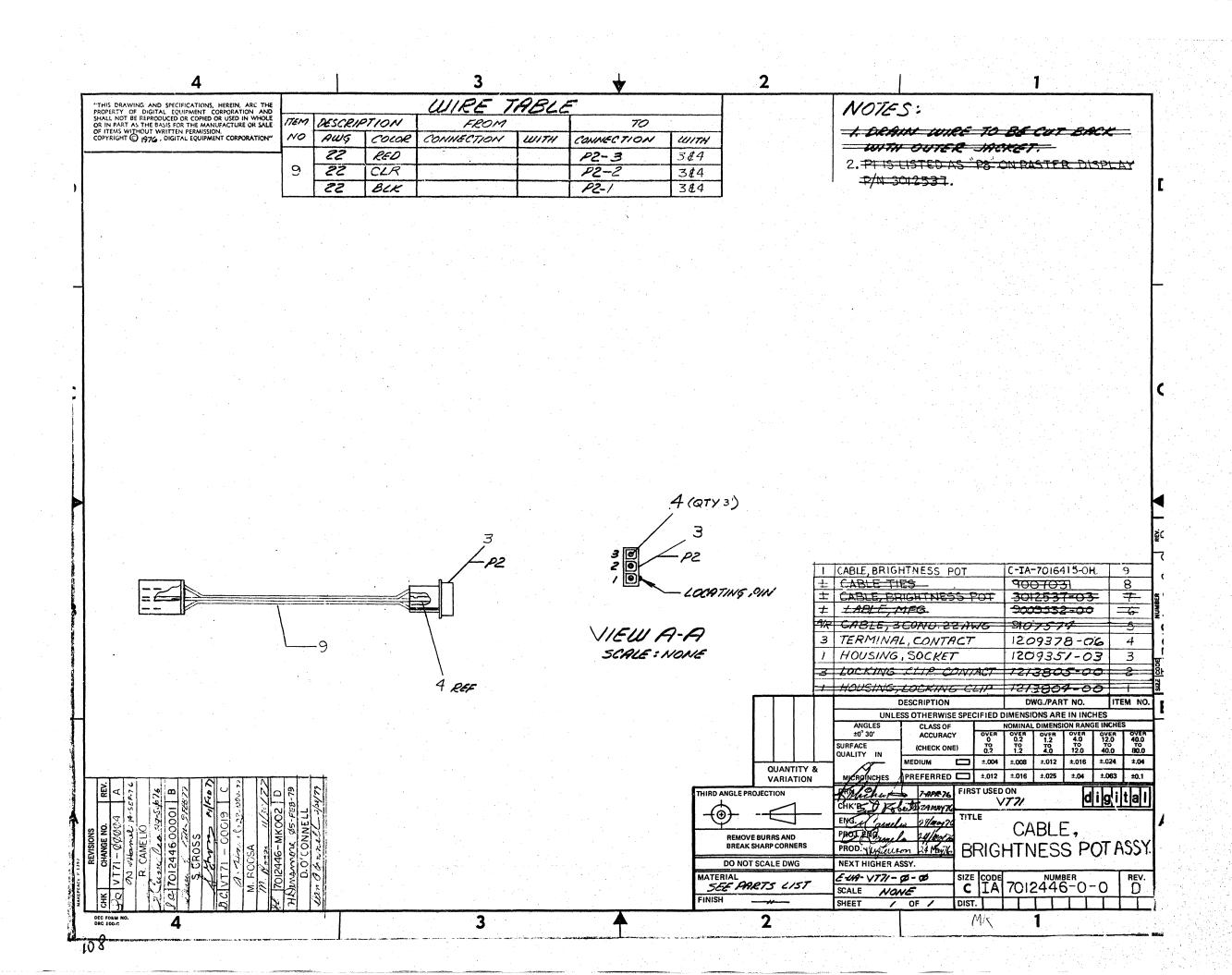


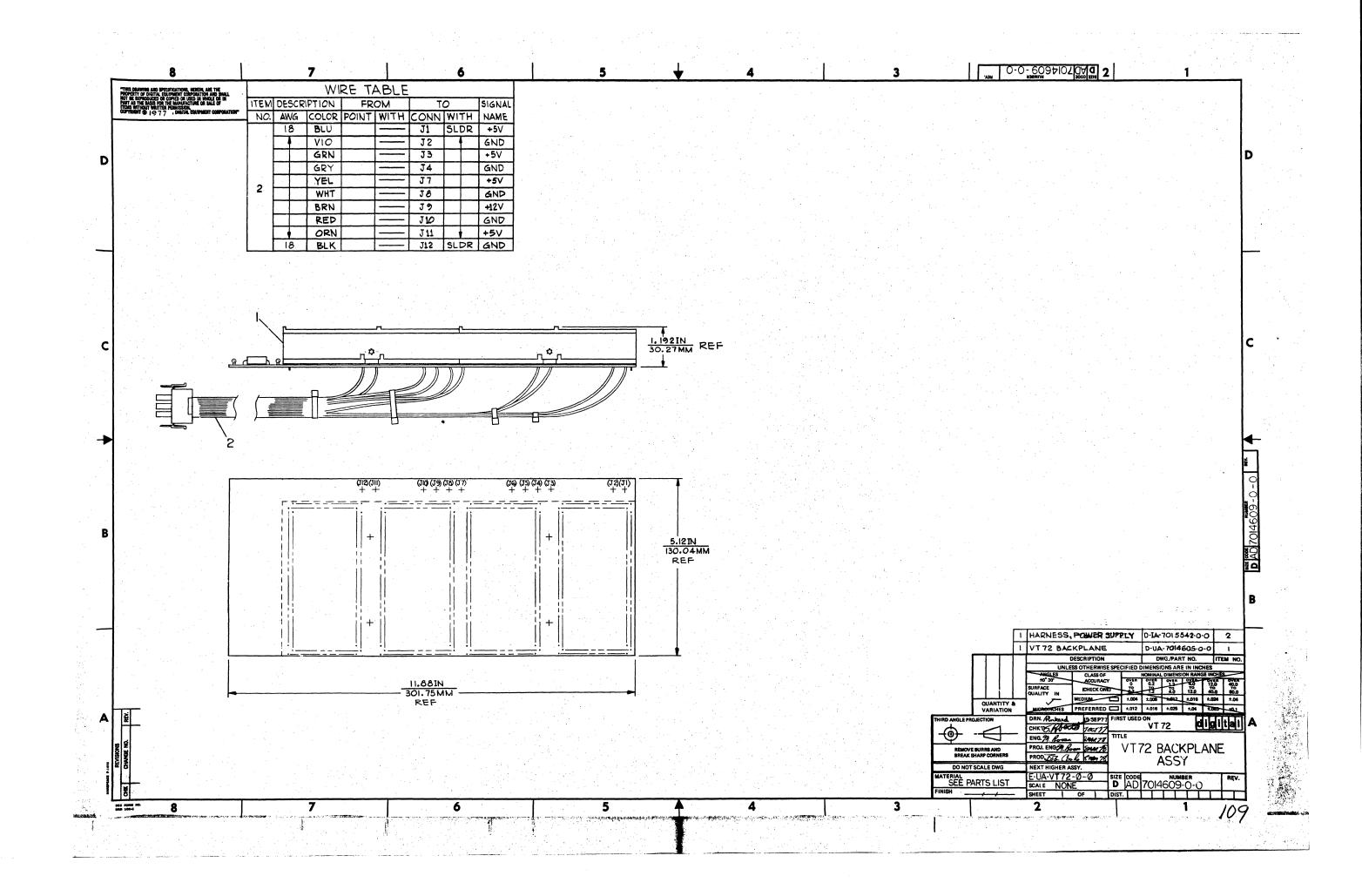


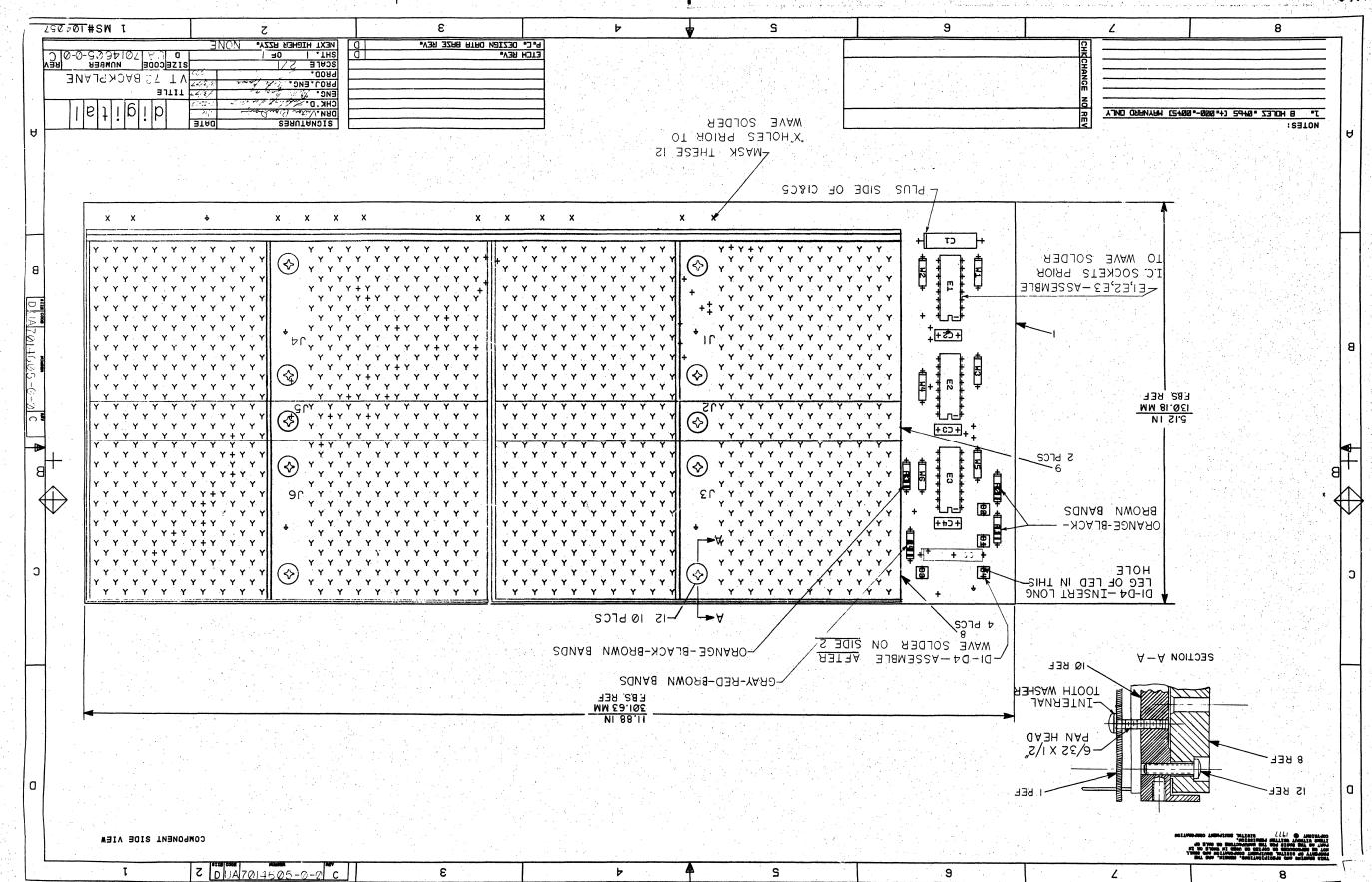


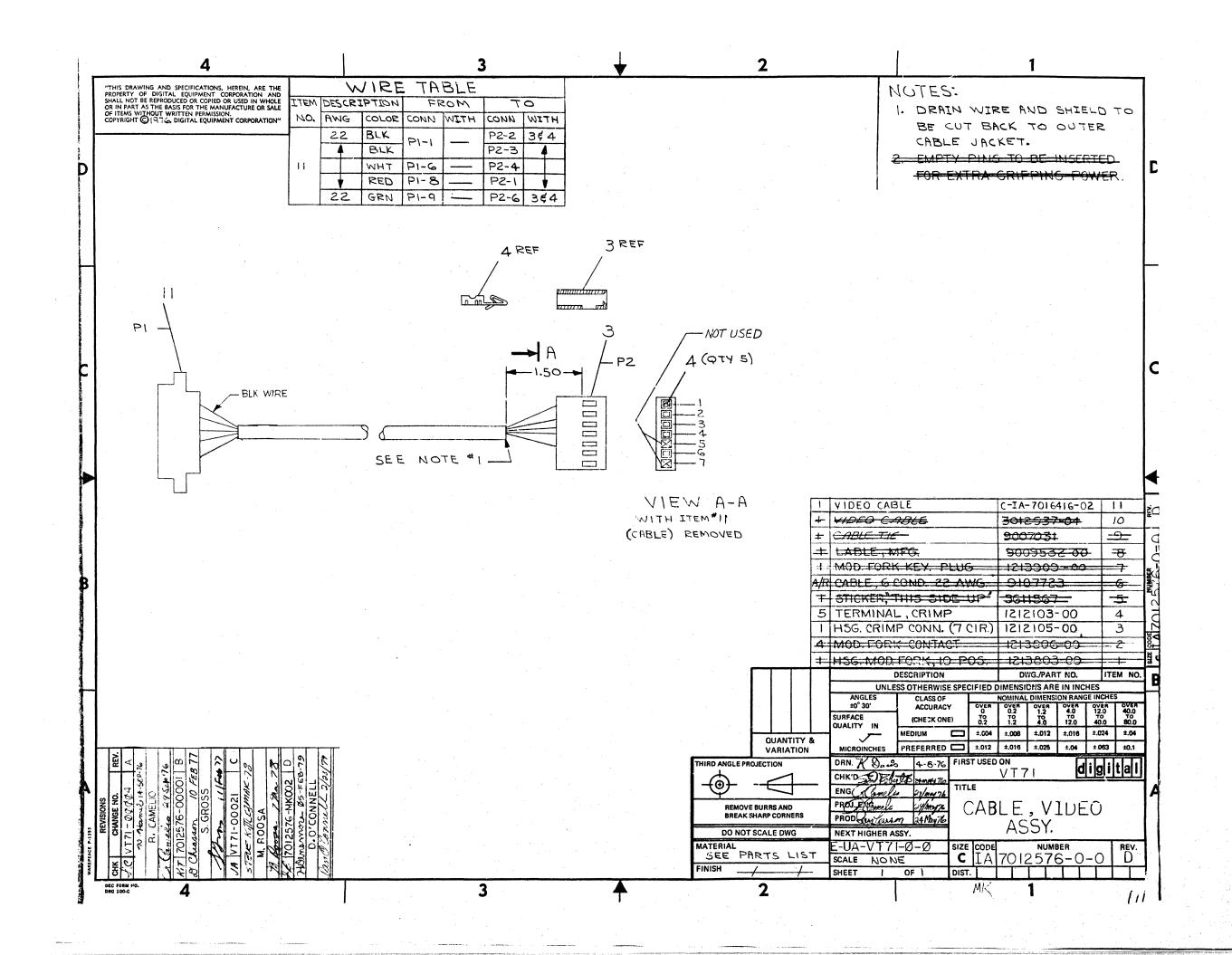












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ENG	INEERING SPECIFICAT	ION			DATE 4/4/	78
TITLE	VT72/t ACCEPTANCE PROCE	DURE - FA &	T			
		REVISIONS				
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
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SHEET _1_ OF __12

CONTINUATION SHEET

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TLE	VT72	/t ACCEPTANCE PROCEDURE - FA & T
2.0	Refe	rence Documents
	2.1	VT72/t Service Manual; (EK-VT72t-SV).
	2.2	VT72/t Print Set.
	2.3	Mast Phase 1 Check Off List.
	2.4	Workmanship Manual; (DEC STD 116).
	2.5	Finish and Color Standard; (DEC STD 092).
3.0	<u>VT72</u>	/t OFF-LINE SELF TEST DIAGNOSTICS
	3.1	Checkout Inspection
		Following receipt of the test item(s), perform a brief (quick scan) visual inspection for obvious discrepancies per the DEC STD 116 and DEC STD 092.
	3.2	Off-Line Checkout
		Run terminal off-line self test step 1, step 2, step 3 and step 4 as defined in chapter 2.4 of the VT72/t Text Editing Terminal Service Manual.
4.0	On-L	ine Test
	4.1	PDP-11 With DHll Interface:
		Go to Section Five(5) for checkout and acceptance procedure.
	4.2	PDP-11 With DL11 Interface:
•		Go to Section Six(6) for checkout and acceptance procedure.
	4.3	PDP-8 With KL8-J Interface:
		<pre>Gc to Section Seven(7) for checkout and acceptance procedure.</pre>
2 - 5 2 5 - 5		
	4.4	PDP-8 With KL8-A Interface:
	4.4	PDP-8 With KL8-A Interface: Go to Section Eight(8) for checkout and acceptance procedure.
	4.4	Go to Section Eight(8) for checkout and acceptance

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ENGINEERING SPECIFICATION

ENGINEERING SPECIFICATION CONTINUATION SHEET VT72/t ACCEPTANCE PROCEDURE - FA & T 1.0 Scope This procedure details the procedure to accept a VT72/t at the system integration or option order area. This procedure details the required procedures to system test a VT72/t on the following system types: 1. PDP-11 with DHl1 interface. 2. PDP-11 with DL11 interface. 3. PDP-8 with KL8-J interface. 4. PDP-8 with DH8-E interface. This procedure is set up in the following manner: SECTION 1 SCOPE SECTION 2 REFERENCE DOCUMENTS SECTION 3 VT72/t OFF-LINE SELF TEST DIAGNOSTICS SECTION 4 ON-LINE TEST SECTION 5 SECTION 6 SECTION 7 SECTION 8 PDP-11 WITH PDP-8 WITH PDP-11 WITH PDP-8 WITH DL11 DH8-E KL8-J REV NUMBER SHEET 2 OF 12 DEC FORM NO EN-01022-16-N370-(381) DRA 108

ENGINEERING SPECIFICATION CONTINUATION SHEET VT72/t ACCEPTANCE PROCEDURE - FA & T 5.0 PDP-11 With DH11 Checkout And Acceptance Procedure 5.1 Required Test Equipment 5.1.1 PDP-11 System With DH11 5.1.2 H319 And BC03S Cable 5.1.3 MRV11-VC = (M7942-YC) 5.2 Required Test Software 5.2.1 MAINDEC-11-DZDHJ, DH11 Echo Cable Test. 5.3 On-Line Test Set-Up Set-up the test item(s), with all power off, in the configuration shown in Figure 1 and insert MRV11-VC into the VT72/t as per service manual, (Appendix A). 5.4 On-Line Checkout And Acceptance If an MRV11-VC is available for each VT72/t to be on-line, system tested do step 5.4.1 (Do not perform step 5.4.2). If an MRV11-VC is $\underline{\text{not}}$ available for each VT72/t to be tested do step 5.4.2. (Do not perform step 5.4.i). 5.4.1 Run ESC, D DLV11 Host Loopback. (See VT72/t Service Manual Section 3.2.3 for details). 5.4.2 Using the steps outlined below, "hand toggle" the following program into the VT72. (On the VT72 keyboard, "NEW PARA" is equivalent to line feed). Instruction Loc Type (LF) 200 (Cmd. to open 105737 Mem. Loc 200) 177650 (LF) 100375 113737 (LF) (LF) 177652 (LF) 771 (CR)

DEC FORM NO EN-01022-16-N370-(381) DRA 108 VT72-Ø-5

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NUMBER

SIZE CODE

ENGINEERING SPECIFICATION CONTINUATION SHEET VT72/t ACCEPTANCE PROCEDURE - FA & T 5.4.3 Load the DH11 Echo Cable Test (MAIN-DEC-11- $\mathtt{DZDHJ})\,.$ Then patch the line parameters register constant to enable even parity. LOC BEFORE AFTER 4620 33503 33523 Then start the test in the host, (LINE SPEED MUST BE 9600 BAUD). 5.4.4 Select the cable test section of the diagnostic. 5.4.5 Allow the test to run for 15 min. on each VT72/t, 5.4.6 No errors are acceptable in the 5.4.5 15 min. per terminal test. 5.4.7 Set bootstrap function switches on the M8656 module. SW #7 of El6 to OFF and SW #8 of El6 to ON. (Further details, see VT72/t Service Manual, Appendix B, Figure B-8). 6.0 PDP-11 With DL11 Checkout And Acceptance Procedure 6.1 Required Test Equipment 6.1.1 PDP-11 System with DL11 6.1.2 H319 and BC03S Cable 6.1.3 MRV11-VC = (M7942-YC) 6.2 Required Test Software 6.2.1 MAIN-DEC-11-DZDLA, DL11 Test. 3.3 On-Line Test Set-Up

Set-up the test item(s), with all power off, in the configuration shown in Figure 2 and insert MRV11-VC into the VT72/t as per service manual, (Appendix A). NUMBER VT72-Ø-5 DEC FORM NO EN-01022-16-N370-(381) DRA 108 SHEET _5 OF _12 **ENGINEERING SPECIFICATION** didgiitia CONTINUATION SHEET TITLE VT72/t ACCEPTANCE PROCEDURE - FA & T

7.4.1 If each VT72/t to be tested has an MRV11-VC,

7.4.2 If each VT72/t to be tested does \underline{not} have an MRV11-VC, perform section 5.4.2.

7.4.4 Allow the test to run for 15 min. on each VT72/t.

7.4.5 No errors are acceptable in the 7.4.4 15 min.

7.4.6 Set bootstrap function switches on the M8656 module. SW #7 of El6 to OFF and SW #8 of El6 to ON. (Further details, see VT72/t Service

Manual, Appendix B, Figure B-8).

8.2.1 MAIN-DEC-8-DJKLA, KL8-A Loopback Test.

Set-up the test item(s), with all power off in the configuration shown in Figure 4 and insert MRV11-VC into the VT72/t as per service manual, (Appendix-A).

7.4.3 Load and start the KL8-J Loopback Test,

7.4 On-Line Checkout And Acceptance

perform section 5.4.1.

(MAIN-DEC-8-DIKLA).

per terminal test.

8.0 PDP-8 With DH8-E Checkout And Acceptance Procedure

8.1.1 PDP-8 System with DH8-E. 8.1.2 H319 and BC03S Cable.

8.1 Required Test Equipment

8.2 Required Test Software

8.4 On-Line Checkout And Acceptance

8.3 On-Line Test Set-Up

6.4.1 If each VT72/t to be tested has an MRV11-VC; perform section 5.4.1. 6.4.2 If each VT72/t to be tested does not have an MRV11-VC; perform section 5.4.2. 6.4.3 Load and start the DL11 Test, (MAIN-DEC-11-DZDLA). Line speed must be 9600 baud. 6.4.4 Select test #56 of the DL11 diagnostic. 6.4.5 Allow the test to run for 15 min. on each VT72/t. 6.4.6 No errors are acceptable in the 6.4.5 15 min. per 6.4.7 Set bootstrap function switches on the M8656 module. SW #7 of El6 to OFF and SW #8 of El6 to ON. (Further details, see VT72/t Service Manual, Appendix B, Figure B-8). 7.0 PDP-8 With KL8-J Checkout And Acceptance Procedure 7.1 Required Test Equipment 7.1.1 PDP-8 System with KL8-J 7.1.2 H319 and BC03S Cable 7.1.3 MRV11-VC = (M7942-YC). 7.2 Required Test Software 7.2.1 MAIN-DEC-8-DIKLA, KL8-J Loopback Test. 7.3 On-Line Test Set-Up Set-up the test item(s), with all power off, in the configuration shown in Figure 3 and insert MRV11-VC $\,$ into the VT72/t as per service manual, (Appendix-A). SIZE CODE SP NUMBER VT72-Ø-5 DEC FORM NO EN-01022-16-N370-(381) DRA 108 SHEET _6_ **ENGINEERING SPECIFICATION**

ENGINEERING SPECIFICATION

VT72/t ACCEPTANCE PROCEDURE - FA & T

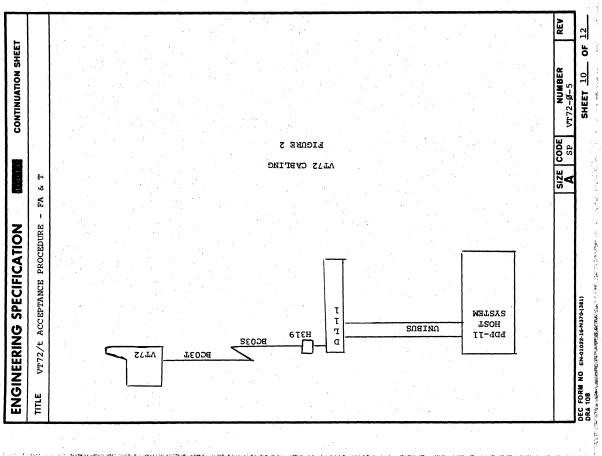
6.4 On-Line Checkout And Acceptance

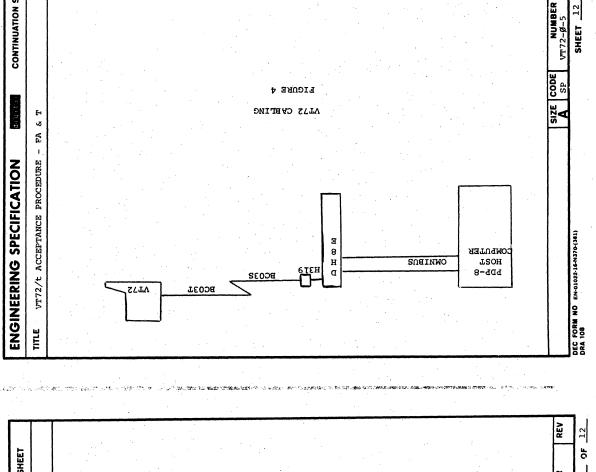
CONTINUATION SHEET

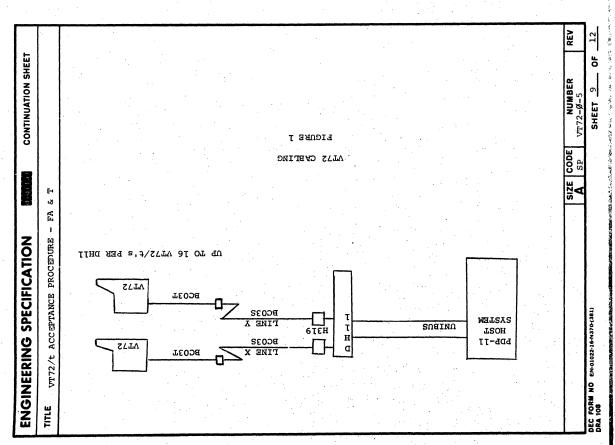
CONTINUATION SHEET VT72/t ACCEPTANCE PROCEDURE - FA & T 8.4.2 If each VT72/t to be tested does \underline{not} have an MRV11-VC, perform section 5.4.2. 8.4.3 Load and start the KL8-A Loopback Test, (MAIN-DEC-8-DJKLA). 8.4.4 Allow the test to run for 15 min. on each VT72/t. 8.4.5 No errors are acceptable in the 8.4.4 15 min. per terminal test. 8.4.6 Set bootstrap function switches on the M8656 module. SW #7 of El6 to OFF and SW #8 of El6 to ON. (Further details, see VT72/t service manual, Appendix B, Figure B-8). SIZE CODE DEC FORM NO EN-01022-16-N370-(381) DRA 108 SHEET _8

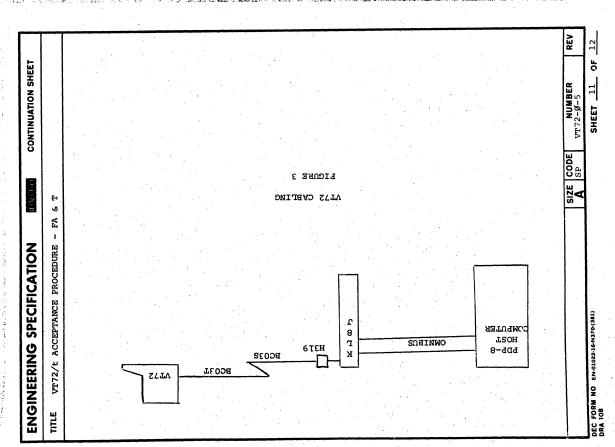
8.4.1 If each VT72/t to be tested has an MRV11-VC. perform section 5.4.1 NUMBER VT72-Ø-5 DEC FORM NO EN-01022-16-N370-(381) DRA 108 SHEET _7 OF 12

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